

Global Memory Market

NAND Flash Memory: Evolution, Current Innovations and Future Outlook

- Long-term NAND dynamics: TAM growth acceleration in the next three years from long-term average of 10%.** Tracing NAND dynamics over the past 25 years, we have seen bit demand growth decelerating on maturing end applications, compensated by slowing ASP decline. Surging eSSD demand is shifting the TAM growth profile from sub-10% to 30+% (next three years' CAGR, per JPMe). Layer migration enables greater bit productivity and cost reduction vs DRAM, but poor margin economics in the past few years limits suppliers from undertaking aggressive capacity expansion, thus we see disciplined capex spending. *NAND unit economics are on a clear improvement trajectory, and we forecast NAND revenue per KwfpM to move up steadily to US\$102k by 2027E* from US\$55k in 2025E or US\$34k five years ago.
- NAND becoming AI enabler with rising eSSD consumption for inferencing.** After its initial demand boom during the 2016-'18 datacenter capex cycle (bit mix: 8% in '15 to 18% in '18), we have witnessed continued above-industry eSSD demand growth (+31% vs industry at +22%) throughout last year ('18-25E). With AI inference driven storage demand proliferation and several new technical approaches to address KV Cache offloading (i.e. context memory storage), *we expect substantial eSSD content growth acceleration in the next 3 years to 900EB* (eSSD bit demand CAGR of +49% from 25E-28E or bit mix 53% by 28E, per JPMe). We are also witnessing a positive SSD demand tailwind from HDD supply tightness, incentivizing QLC-based nearline storage adoption. *We expect both HDD and SSDs to complement each other in different segments* (HDD for affordable/large-scale storage vs SSD for speed-sensitive tasks).
- NAND vs DRAM comparison.** Investors find NAND less attractive vs DRAM due to : 1) market fragmentation (incl. stronger China presence, 2) higher exposure to consumer electronics, and 3) lower exposure to AI. We view NAND suppliers' capex discipline as stricter (25E-27E capital intensity average at 16% vs 26% for DRAM) and find key suppliers' strategic DRAM focus makes clean room constraints worse in the mid to long term. It is worth noting that *the AI NAND TAM CAGR remains higher vs AI DRAM TAM CAGR* (25E-27E) upon robust enterprise SSD growth. We estimate a US\$70bn AI NAND TAM (value) by 2028E (vs AI DRAM TAM of US\$220bn).
- Historical NAND dollar value comparison.** NAND represented 4%/11% of consumer electronics (Smartphones/NBPCs) device prices and 5% of average server prices during the past peak cycle in 2015-25E. Following the surge in NAND prices, we estimate the value mix to be different across applications: i) smartphone: surpassed the peak, leaving limited room for price hike, ii) PC: slightly below the peak with nearly 10% room for price hikes, iii) server: substantially below the peak (rising AI server mix and increase in BOM mostly centered around HBM, GPU, power, and other electronic components, but less on NAND). *Upside to CE-grade NAND ASP is likely to be capped by year-end, however, we see ample room for upside to enterprise server* (p32 for details).

Technology - Semiconductors

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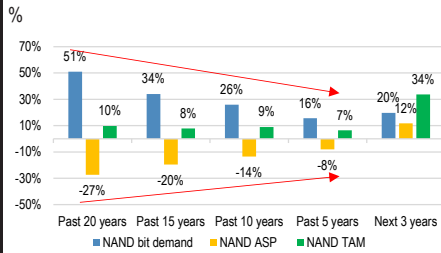
- **Technology migration leads to capacity shrink, HBF could be a wild card in the long term.** Layer/stacking migration results in a natural NAND wafer input capacity shrink over time. As TSV/stacking related tool intensity rises and memory makers allocate incremental cleanroom space to DRAM, we expect to see NAND cleanroom area share continuously declining at major memory makers. *We expect such “capacity shrink and migration-driven production maximization” strategies to continue in the foreseeable future*, alongside CMOS-bonded-to-Array architecture adoption increase. HBF (High-Bandwidth Flash) is still at the proof of concept stage, but *we believe successful commercialization in the future (earliest likely 2028, in our view) could be positive for industry S-D, due to higher wafer die penalty vs normal 3D NAND die.*
- **How to trade NAND stocks?** Key share price drivers (pricing momentum, AI DC hardware buildout and related storage demand prospects, and supply/production updates) are similar between NAND and DRAM (p5-7 for details). *We find a stronger and longer upcycle view is a generally applicable principle even for NAND and convey a multi-year constructive view. Consumer demand erosion remains a risk point, but we expect growing eSSD mix to help weather the potential down-cycle.* We like **Kioxia** (OW view [initiation](#)) as a pure NAND play in the Asian memory space, based on the above-industry server mix expansion growth profile. In the broader memory space, we continue to like **SEC**, **SKH**, **Winbond** (OW, covered by Jimmy Huang), and **SIMO** (OW, covered by Gokul Hariharan). Within the Asia SPE space, we like Tokyo Electron (OW, covered by Mio Shikanai).

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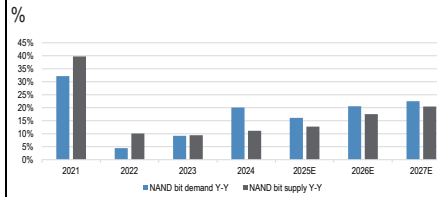
Killer Charts

Figure 1: LT NAND industry trends



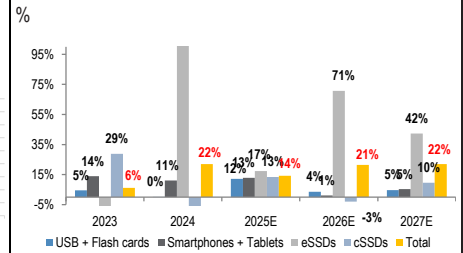
Source: Company reports, J.P. Morgan estimates.

Figure 2: NAND industry demand vs supply growth



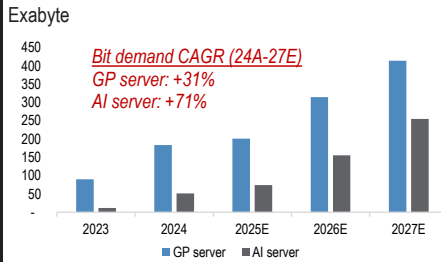
Source: WSTS, J.P. Morgan estimates.

Figure 3: NAND demand growth



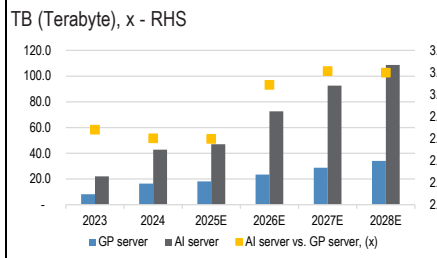
Source: Omdia, J.P. Morgan estimates. J.P. Morgan estimates. Note: eSSD growth of 130% in 2024 has been truncated.

Figure 4: eSSD GP server vs AI server bit demand comparison



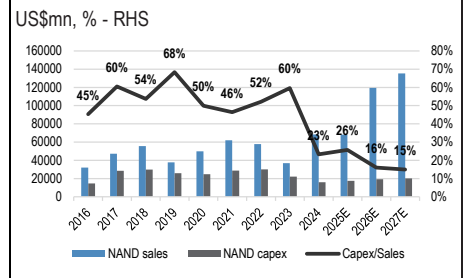
Source: IDC, Gartner®, J.P. Morgan estimates.

Figure 5: Storage content difference between GP and AI server



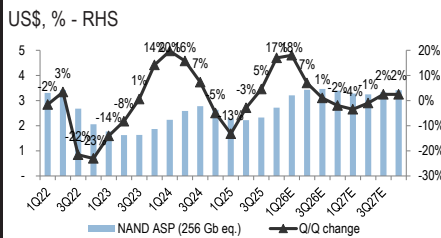
Source: Gartner®, J.P. Morgan estimates.

Figure 6: NAND capex to sales



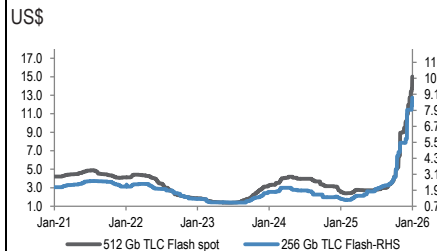
Source: Company reports, J.P. Morgan estimates.

Figure 7: NAND ASP trend



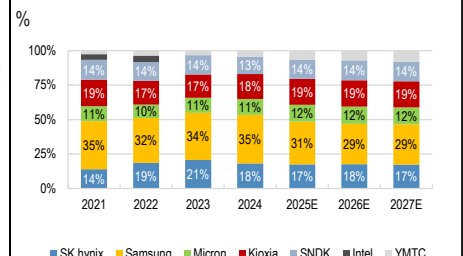
Source: WSTS, J.P. Morgan estimates

Figure 8: NAND spot/contract trend



Source: Bloomberg Finance L.P.

Figure 9: NAND market share trend



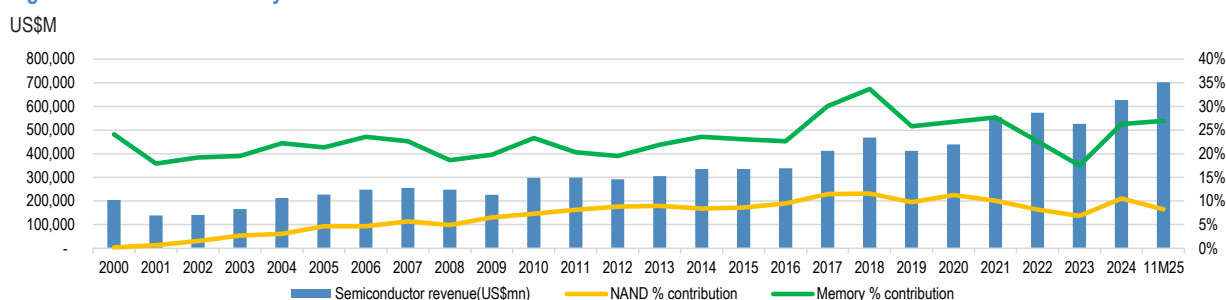
Source: Gartner®, J.P. Morgan estimates.

Long-Term NAND Market Dynamics

NAND flash was introduced as a non-volatile, high-density, lower-cost per bit alternative for bulk storage, and the first commercial launch of NAND flash memory can be traced back to 1987. While its limited memory capacity hindered its widespread adoption in the early 1990s, the *rise of portable electronic devices, such as digital cameras, smartphones and MP3 players*, coupled with the need for efficient and scalable storage solutions, led to increased adoption of NAND flash as it offered a cost-effective solution compared to other types of storage, such as DRAM.

NAND has grown immensely over the past 25 years, accounting for ~10% of the total semiconductor market (memory, including DRAM and NAND, accounts for over 25% of the semiconductor market), according to WSTS. Over the last 25 years, the expansion in both unit sales and content per device across traditional platforms such as mobile phones, PCs, and notebooks, along with the rise of new demand drivers, such as data centers and AI servers, has led to fundamental growth in the NAND market.

Figure 10: NAND and memory % contribution to total semiconductor market



Source: WSTS. Note: For 2025, we have taken data for 11 months from Jan-Nov'25.

Long-term NAND bit demand and ASP CAGR

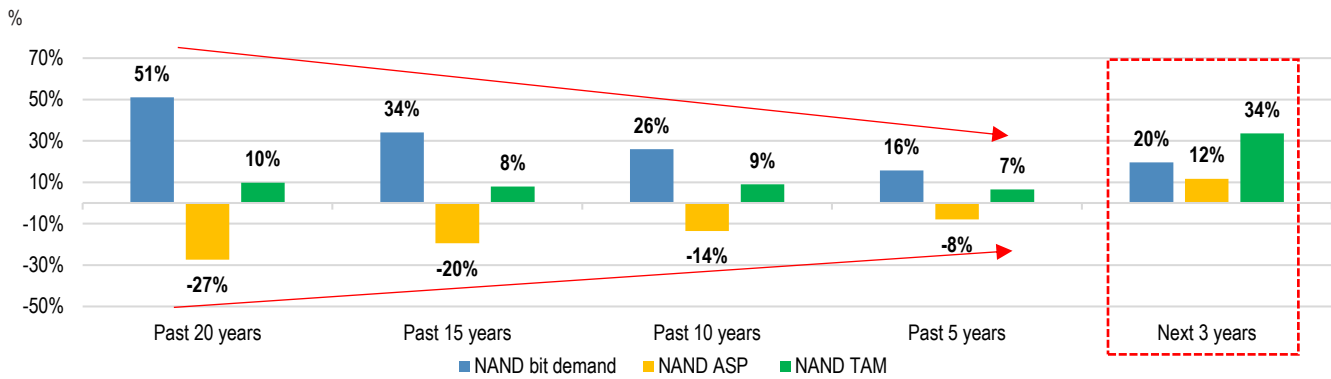
Tracking NAND history over the last 25 years, we observe that the pace of growth in NAND bit demand has slowed over time as end markets such as smartphones and PCs have matured following their rapid adoption in their early years, while consumers are reluctant to make storage upgrades. Likewise, bit density per die has improved via 3D NAND scaling, which further accelerated bit growth. On the ASP front, historically, lower ASPs drove strong bit growth, however, now demand is less elastic to price as the additional cost savings are being used to upgrade other high end chips, rather than doubling NAND capacity. Nonetheless, despite a structural deflationary trend in ASP, coupled with a decline in the pace of growth of bit demand, the NAND TAM has grown at a low-teens % CAGR over the last 25 years.

Over the years, the NAND market has been driven by multiple end demand drivers, starting with USB & flash cards, which drove the majority of bit demand in the early 2000s, followed by the introduction of smartphones in 2009-10. Following the financial crisis, the NAND industry saw 10 years of consecutive Y/Y growth from 2009-2018, with annual smartphone shipments rising from 173mn in 2009 to 1.5bn in 2018 (27% CAGR), while smartphone content growth rose from 4850MB in 2009 to 56650MB in 2018 (31% CAGR). However, from 2018-'25, while the pace of NAND content growth has declined, unit shipments have also declined, after peaking in 2017.

Interestingly, within these cycles, SSDs emerged as a structural growth driver, initially with client SSDs (for PC) in the 2010s, followed by enterprise SSDs (for Server). *Of note, as of 2024, SSDs account for 54% of NAND bit demand, while smartphones occupy ~30% with other applications accounting for the remaining 16%.* Moving forward, as AI and accelerated computing drive demand for low cost, high performance storage, we expect SSDs to account for the majority of NAND bit demand, driven by both content growth as well as unit shipments, while smartphone demand continues to be mainly driven by content growth rather than unit shipments.

On a blended basis, following 20 years of deflationary pricing, we expect NAND TAM to expand by a 34% CAGR over the next three years, mainly driven by a 20% bit demand CAGR, coupled with NAND ASP rising by low-teens % over the next three years – an unprecedented trend since the introduction of NAND flash.

Figure 11: Long-term NAND bit demand, ASP, and TAM CAGR



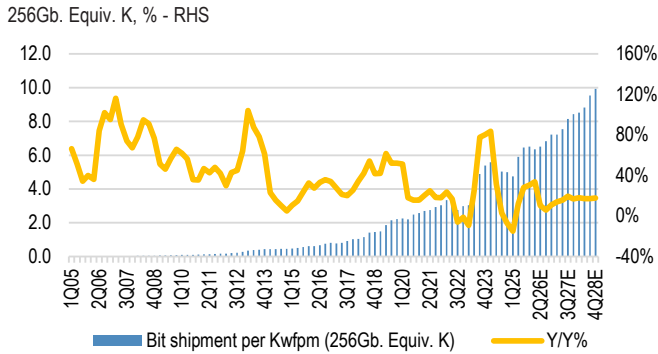
Source: WSTS, J.P. Morgan estimates.

Long-term NAND bit supply and ASP trends

The structural deflationary trend of NAND ASP can be observed from the increasing NAND bit shipments per Kwfp (proxy for NAND bit output per Kwfp) which have been on an upward trend in the past 25 years. Traditionally, memory has been viewed as a commodity product where cost efficiency by each supplier (or the layer count that dictates cost/bit) drove memory makers to accelerate capacity expansion (to enjoy economies of scale) and layer count migration (to improve profitability).

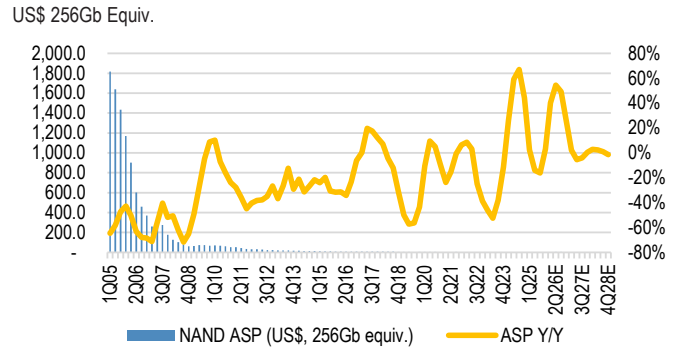
Likewise, the transition from planar NAND to 3D NAND technology has enabled the stacking of memory cells vertically, increasing storage capacity without a proportional increase in cost, further putting pressure on ASP. While bit shipments per Kwfp have plateaued in the ~5k range over the last 2 years, we expect bit shipments per Kwfp to rise beyond the 5k range in the next two years, mainly driven by bit shipment growth amidst limited capacity additions by NAND makers, as inventory across the supply chain remains broadly healthy.

Figure 12: Long-term NAND bit shipments per Kwfp



Source: Company data, J.P. Morgan estimates.

Figure 13: Long-term NAND ASP trend

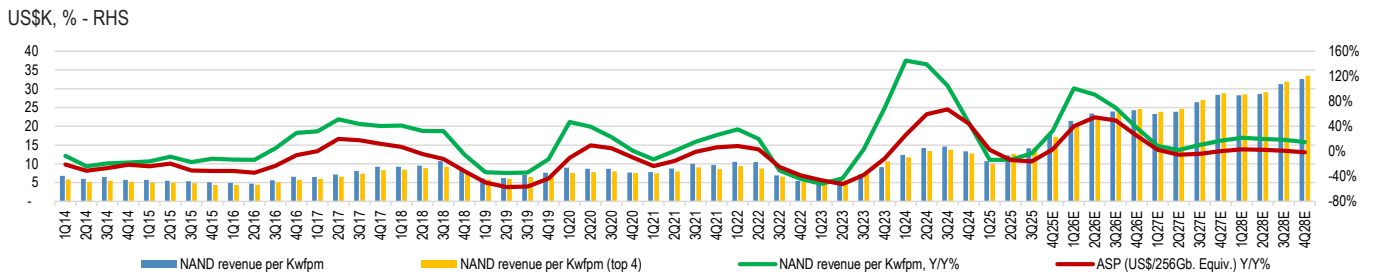


Source: WSTS, company data, J.P. Morgan estimates.

Long-term NAND revenue per Kwfp

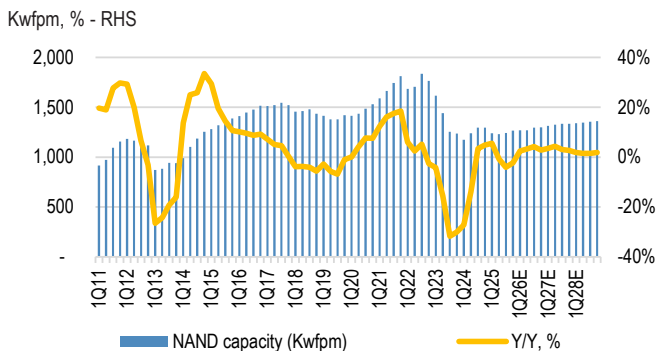
Plotting NAND revenue per Kwfp (or NAND wafer blended ASP), we note that NAND wafer prices moved broadly similarly to the NAND ASP trend. While NAND wafer prices per Kwfp peaked at ~US\$14.6K during the server upcycle in 3Q24, mainly driven by the accelerated adoption of eSSDs in the datacenters by hyperscalers, we expect the NAND wafer price per Kwfp trend to accelerate sequentially from 1Q25-4Q26E as NAND ASPs rise sequentially, driven by strategic production cuts by major manufacturers and strong demand from AI-driven data centers for high-capacity enterprise SSDs.

Figure 14: NAND revenue per Kwfp



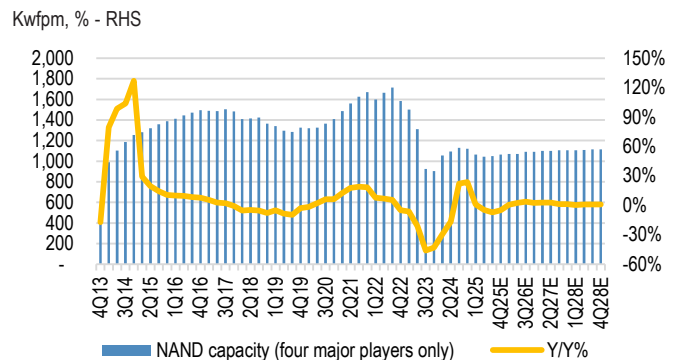
Source: WSTS, company data, J.P. Morgan estimates.

Figure 15: NAND capacity trend



Source: Company data, J.P. Morgan estimates.

Figure 16: NAND capacity trend (four major players only)



Source: Company data, J.P. Morgan estimates.

NAND vs DRAM comparison

DRAM (Dynamic Random Access Memory) is fast, volatile memory (loses data without power) used for active system tasks (like running apps), while NAND Flash is slower, non-volatile storage (keeps data powered off) for long-term storage (SSDs, USBs). Not only do they serve different purposes, but their demand drivers have varied over the last 25 years.

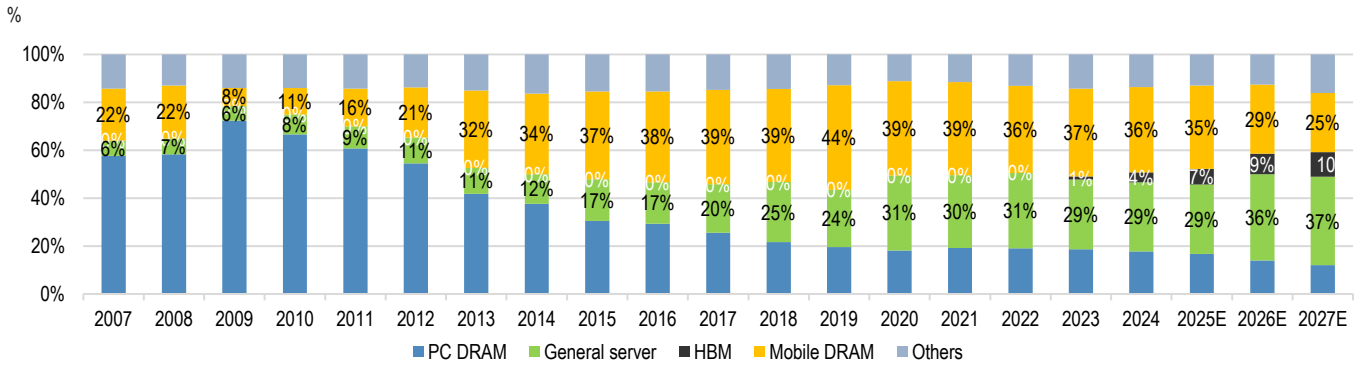
In the DRAM market, manufacturers are increasingly constrained by physical limitations in scaling memory density through front-end node migration. As a result, DRAM bit output per wafer has plateaued at around 5,000 GB per wafer, and the wafer price has struggled to surpass its previous peak of approximately US\$24,000 per wafer, last seen in the third quarter of 2018.

In contrast, the NAND market has benefited significantly from the transition from planar NAND to 3D NAND technology. This shift has enabled manufacturers to stack memory cells vertically, increasing storage capacity without a proportional rise in cost, which has supported average selling prices (ASPs). While NAND bit shipments per thousand wafers per month (Kwfp_m) have plateaued at around 5,000 over the past two years, we expect this figure to rise beyond 5,000 in the next two years. We believe this growth will be driven by increased bit shipments, even as capacity additions remain limited due to healthy inventory levels across the supply chain.

NAND wafer pricing also reflects these dynamics. The price per Kwfp_m peaked at approximately US\$14,600 during the server upcycle in the third quarter of 2024, fueled by accelerated adoption of enterprise SSDs (eSSDs) in data centers by hyperscalers. Looking ahead, we expect NAND wafer prices per Kwfp_m to accelerate further from the fourth quarter of 2025 through the fourth quarter of 2026, as ASPs rise sequentially. This trend will be supported by strategic production cuts from major manufacturers and robust demand from AI-driven data centers for high-capacity enterprise SSDs.

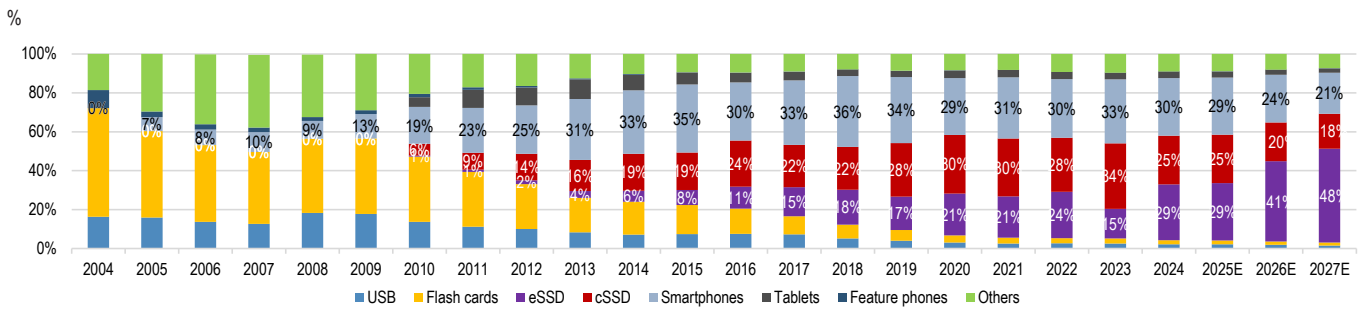
For both DRAM and NAND, bit demand growth has decelerated on maturing end-applications, broadly offset by a slowing ASP/bit decline. However, DRAM TAM growth has been accelerating, especially in the past 20, 10 and 5 years, achieving a DD% growth rate over the past 5 years driven by HBM. However, given NAND's limited participation in AI model training, NAND TAM growth has been decelerating, especially in the past 20, 10 and 5 years, achieving HSD % growth driven by the unprecedented NAND downcycle in 2022-23. However, we expect both DRAM and NAND TAMs to continue to grow higher over the next three years, driven by both bit demand and ASP growth.

Figure 17: DRAM demand contribution by application



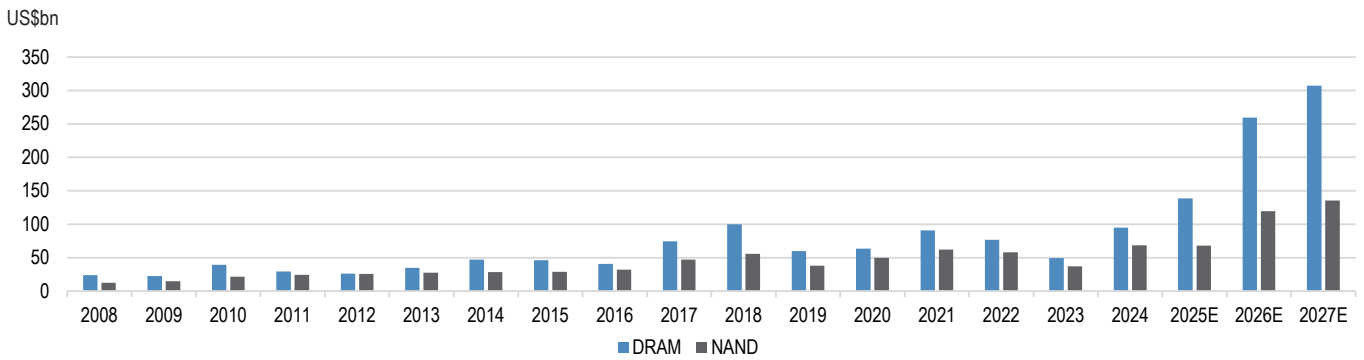
Source: WSTS, J.P. Morgan estimates.

Figure 18: NAND demand contribution by application



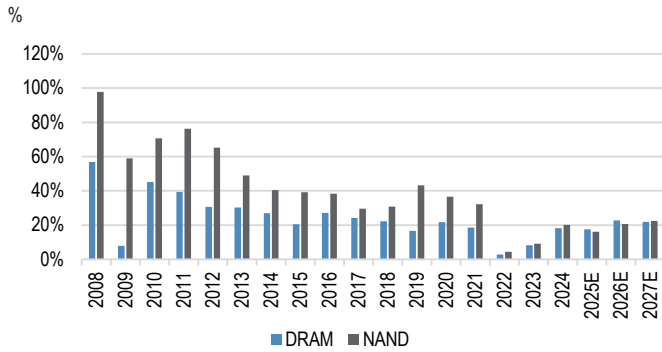
Source: WSTS, J.P. Morgan estimates.

Figure 19: DRAM vs NAND TAM comparison



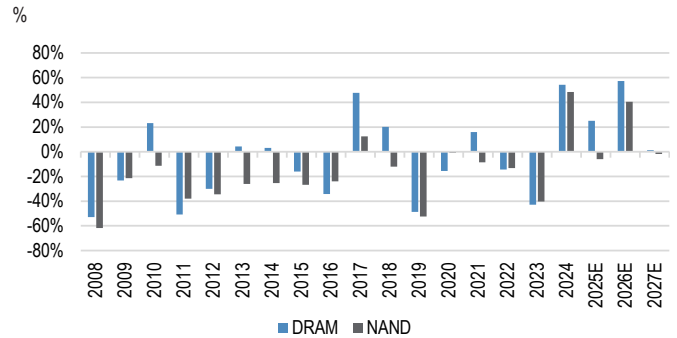
Source: J.P. Morgan estimates, Company data

Figure 20: DRAM vs NAND bit growth y-y comparison



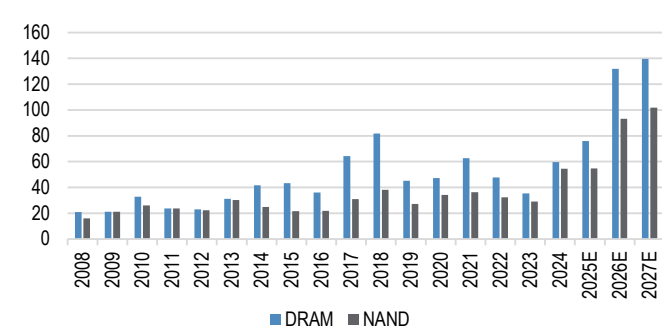
Source: WSTS, J.P. Morgan estimates.

Figure 21: DRAM vs NAND ASP change y-y comparison



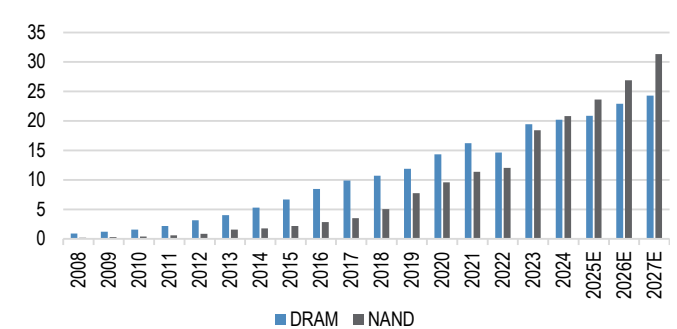
Source: WSTS, J.P. Morgan estimates.

Figure 22: DRAM vs NAND revenue per kwfpm comparison



Source: WSTS, J.P. Morgan estimates.

Figure 23: DRAM vs NAND bit shipment per Kwfpkm comparison



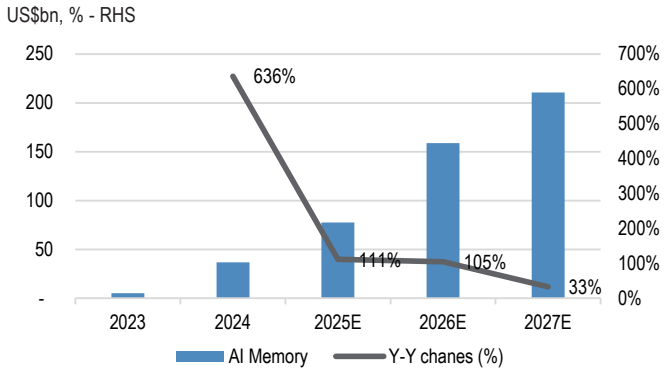
Source: WSTS, J.P. Morgan estimates.

Memory in AI

AI will be nearly half of Global Memory TAM by 2027E (growing at ~80% CAGR during '24-27E), per our estimates. However, AI NAND revenue is substantially smaller than that of AI DRAM (only 1/3 size) as DRAM was the major portion of AI related memory demand pick at the beginning. However, we are witnessing robust NAND demand catch-up driven by strong eSSD demand for AI inferencing. During 2023-2025E, DRAM accounted for 77% to 81% of the total AI memory market (TAM). However, from 2026E-27E, we anticipate a modest decline in DRAM's share, with NAND expected to experience stronger growth and capture a larger portion of the market.

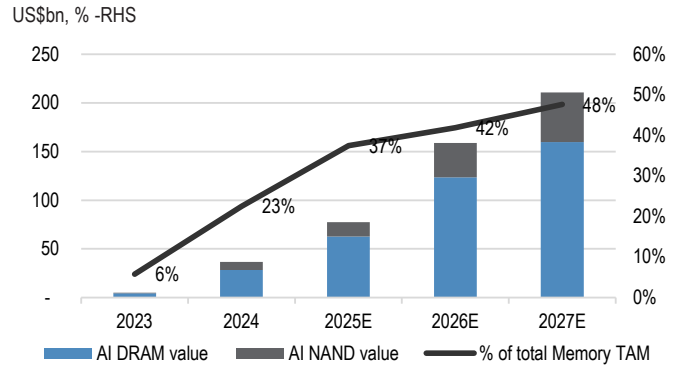
We expect robust growth momentum both in DRAM/NAND throughout 2027E (AI NAND slightly higher than AI DRAM: +83% vs +78%). However, given the ongoing pricing momentum for both DRAM/NAND, we do not rule out the possibility of both memory TAMs' CAGR being revised up in the coming months. It is worth noting that the AI Memory TAM expansion pace is sharper than that of the AI revenue CAGR guidance from leading foundry supplier TSMC (latest guidance at 50%+ CAGR from 2024-29E, communicated during Jan-2026, 4Q25 result call).

Figure 24: AI memory Y/Y trend



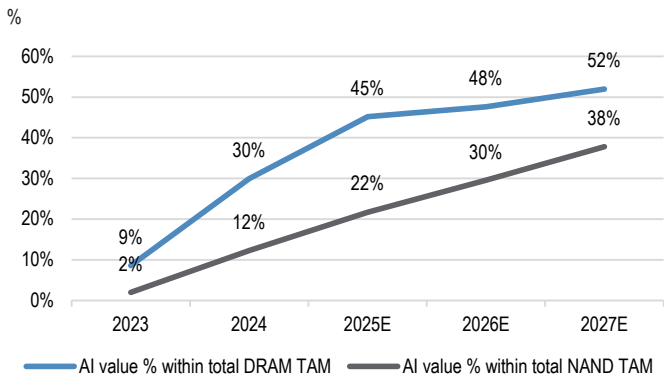
Source: Company reports and J.P. Morgan estimates.

Figure 25: AI DRAM and NAND revenue trend



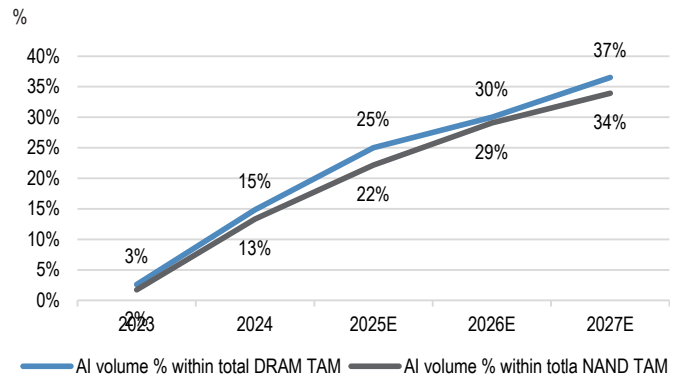
Source: Company reports and J.P. Morgan estimates.

Figure 26: AI value within total DRAM & NAND TAM



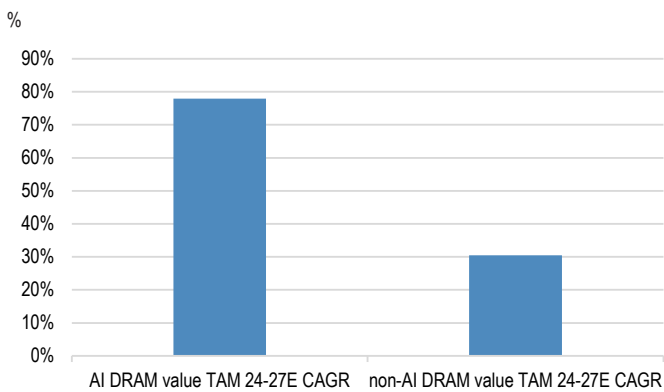
Source: Company reports and J.P. Morgan estimates.

Figure 27: AI volume with total DRAM & NAND TAM



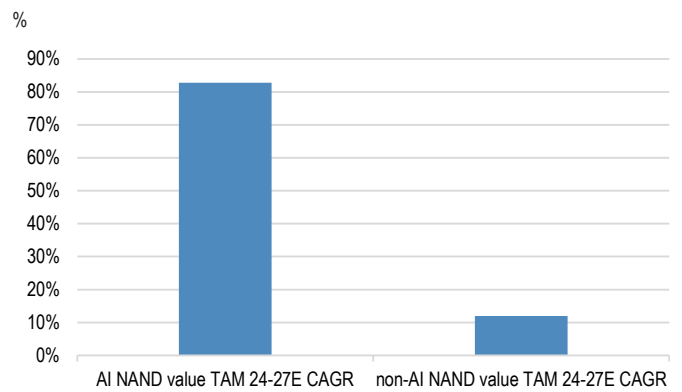
Source: Company reports and J.P. Morgan estimates.

Figure 28: AI and non-AI DRAM value TAM CAGR trend



Source: Company reports and J.P. Morgan estimates.

Figure 29: AI and non-AI NAND value TAM CAGR trend

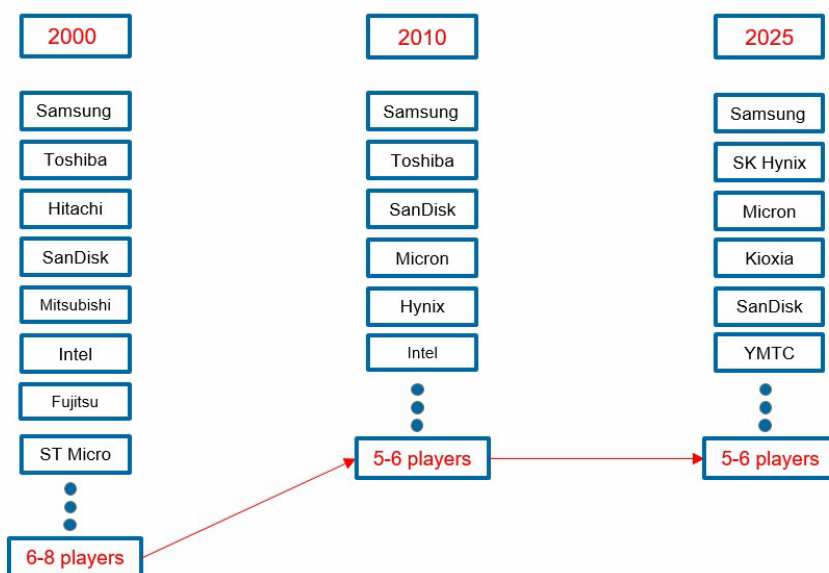


Source: Company reports and J.P. Morgan estimates.

NAND industry structure

Going back to the early 2000s, the NAND industry was mainly driven by rapid innovation, expansion, frequent price wars, and volatile profits with the industry having ~8 key players. However, the boom-bust nature of the NAND industry has led to some consolidation driven by mergers and JVs as smaller players either exited the industry or were acquired by larger players (e.g.- Toshiba-SanDisk, etc.). While the market is currently dominated by a handful of large firms, such as SEC, Kioxia, SKH etc., true consolidation has not fully occurred and pricing cycles and supply gluts continue to take place, competitive dynamics within the industry will persist and game-theory outcomes (where firms act rationally to maximize profits by limiting competition) may not be realized in the near term.

Figure 30: NAND industry consolidation snapshot



Source: J.P. Morgan estimates.

Why has the NAND industry not seen consolidation like DRAM?

The NAND flash memory market has remained less consolidated compared to the DRAM market due to several distinct factors, such as market dynamics, technology, and economic factors. Unlike DRAM, which is highly capital-intensive and standardized (an oligopoly market dominated by a few major players, such as Samsung, Micron, and SK Hynix), the NAND market benefits from a broader range of applications and technological differentiation. This diversity allows for more competition among companies such as Samsung, Kioxia, Western Digital, Micron, SK Hynix, and YMTC, with no single entity exerting overwhelming control.

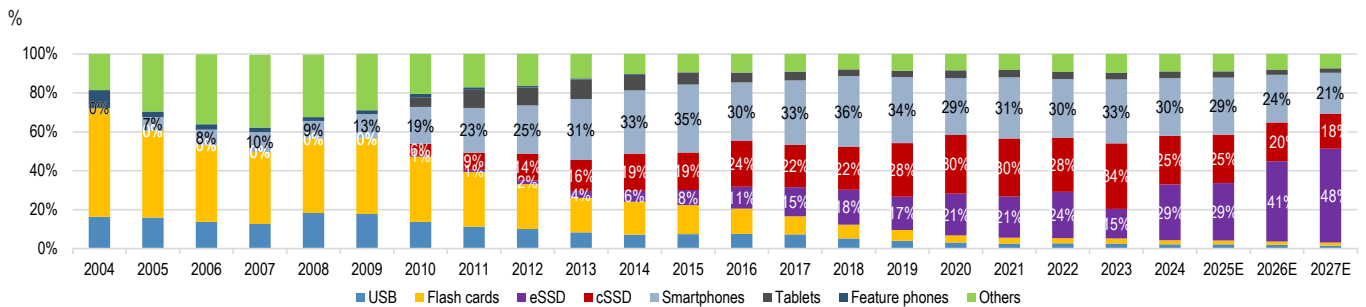
In addition, technological innovations in NAND, such as 3D NAND stacking and controller advancements, enable smaller players to target niche markets, reducing the pressure for consolidation. Additionally, joint ventures and regional diversity, supported by government investments, have sustained a larger number of players in the NAND market. While geopolitical tensions and market dynamics may drive some consolidation in the future, we believe the NAND market's growth and diverse demand will continue to support a competitive landscape distinct from the DRAM sector.

Deeper look into NAND demand dynamics

Key end markets

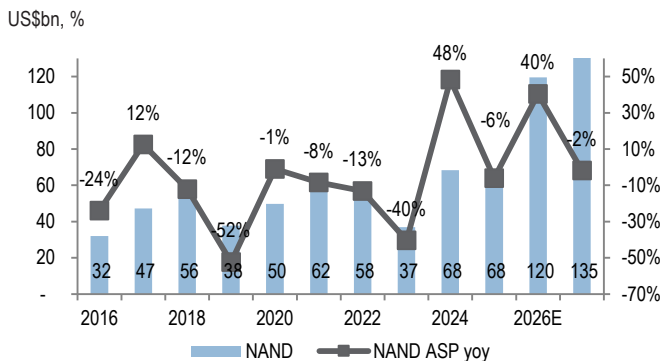
Over the years, the NAND market has been driven by multiple end demand drivers, starting with USB & flash cards, which drove the majority of bit demand in the early 2000s, followed by the introduction of smartphones in 2009-10. Following the financial crisis, the NAND industry saw 10 years of consecutive Y/Y growth from 2009-2018, with annual smartphone shipments rising from 173mn in 2009 to 1.5bn in 2018, while smartphone content growth rose from 4,850MB in 2009 to 56,650MB in 2018. However, over the next 7 years, while the pace of NAND content growth has been rising, unit shipments have been on a decline after peaking out in 2017. Interestingly, within these cycles, SSDs emerged as a structural growth driver, initially with client SSDs in the 2010s, followed by enterprise SSDs. Of note, as of 2025, we estimate that SSDs account for 54% of NAND bit demand, while smartphones occupy ~30%, with other applications accounting for the remaining mid-teens %. Moving forward, as AI and accelerated computing drive demand for low cost, high performance storage, we expect SSDs to account for the majority of NAND bit demand driven by both content growth as well as unit shipments, while smartphone demand continues to be driven mainly by content growth rather than unit shipments.

Figure 31: Application wise contribution % within total NAND



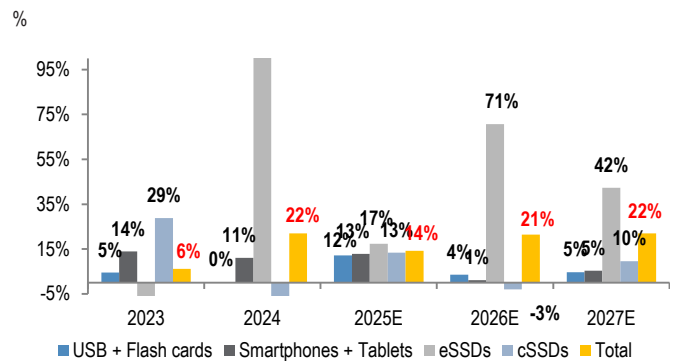
Source: Gartner®, Company data, J.P. Morgan estimates.

Figure 32: NAND market revenue and ASP YoY change



Source: WSTS, J.P. Morgan estimates.

Figure 33: NAND demand growth Y/Y by key application

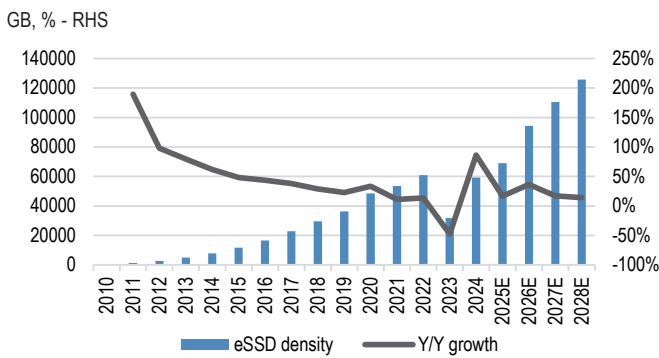


Source: OMDIA, WSTS, J.P. Morgan estimates.
 Note: eSSD growth of 130% in 2024 has been truncated.

eSSD: Opening up growth potential as an AI enabler

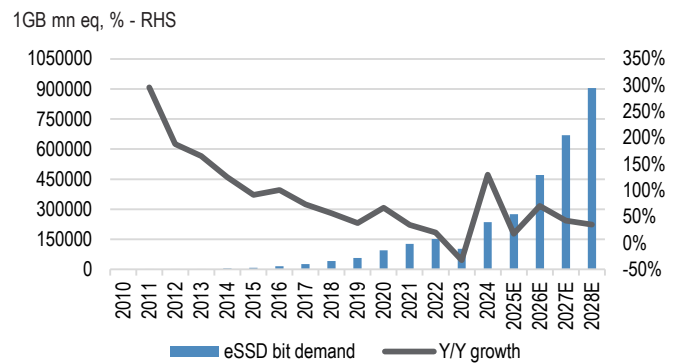
While the broader NAND industry has had limited exposure to the AI and accelerated computing industry until 2023, eSSDs have emerged as a memory solution that combines the speed, reliability, and scalability needed for AI and accelerated computing. The recent, exceptional shortage in bit supply and the sharp rise in ASP have been primarily fueled by the rapid expansion of data centers and AI infrastructure. Hyperscalers, cloud service providers, and AI research labs are rolling out increasingly storage-intensive systems, a trend further intensified by suppliers exercising greater restraint in expanding wafer capacity compared to previous years. To meet the demands of model training, inference workflows, and vast data lakes, large-capacity enterprise SSDs are being adopted ahead of schedule. QLC-based SSDs are becoming a popular nearline storage option over HDDs – where supply is also constrained – thanks to their enhanced endurance, lower cost per bit, and superior energy efficiency. Of note, eSSD shipments rose 86% Y/Y in 2024, a level last surpassed back in Q2012, and we expect them to grow by HSD %/low-teens on average over the next 3 years as AI infrastructure growth continues at an unabated pace.

Figure 34: eSSD LT content growth trend



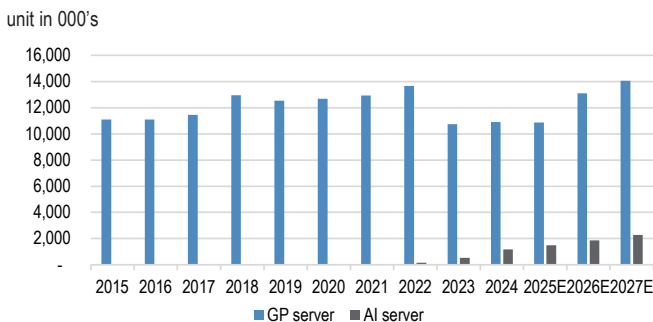
Source: IDC, Gartner®, J.P. Morgan estimates.

Figure 35: eSSD LT bit growth trend



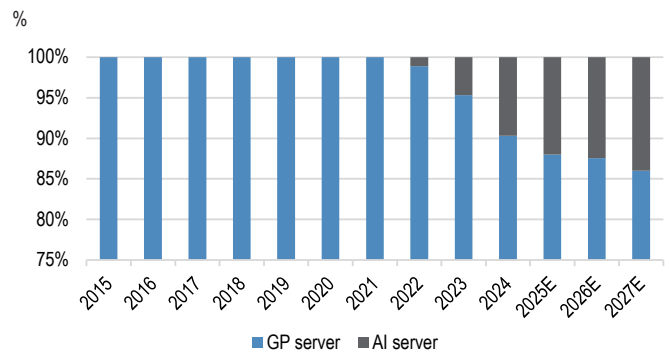
Source: IDC, Gartner®, J.P. Morgan estimates.

Figure 36: Server unit demand by GP vs. AI



Source: IDC, Gartner®, J.P. Morgan estimates.

Figure 37: Server Unit Demand Mix by GP vs. AI



Source: IDC, Gartner®, J.P. Morgan estimates.

Two types of eSSD

Compute eSSD: Compute eSSDs are optimized for high-performance computing tasks and are designed to handle intensive workloads that require fast data processing and low latency. They are characterized by high Input/Output Operations Per Second (IOPS) that enable rapid data access, thereby minimizing latency and providing reliability for critical applications. They are ideal for applications such as databases, virtual machines, and real-time analytics, where performance and speed are crucial.

Storage eSSD: Storage eSSDs are optimized for capacity and data retention and are designed to store large volumes of data efficiently and reliably. Storage eSSDs provide high capacity, cost-effective storage per gigabyte, and robust endurance for reliable long-term data archiving and management. They are suitable for applications such as data warehousing, backup solutions, and content delivery networks, where storage capacity and data retention are key.

NAND in AI training/inference

NAND memory plays a critical role in large language model (LLM) training by providing the high-speed storage necessary to handle massive training datasets. NAND's main value proposition is its *high-capacity, low-cost data storage* for the massive, curated datasets required for training. While NAND is too slow for the real-time parallel processing done by the GPUs with the help of HBM, it is extremely efficient in handling the read-intensive workflow of feeding data to the faster, more expensive DRAM and GPU memory.

In the initial LLM training phase, the model is trained on massive amounts of raw data scraped from the internet, books, and other texts. While DRAM can be used for this, it is extremely expensive and hence NAND based solutions are far more cost-effective for storing these vast datasets.

When it comes to LLM training, the focus is on maximizing the amount of data processed per second (high throughput) while latency (the time to process a single batch) is less critical than overall speed and efficiency. On the other hand, inference often happens in real-time (e.g., responding to a user query) and users expect quick responses, so low latency (fast prediction) is crucial. Throughput (total predictions per second) is less important than how fast each prediction is delivered.

While the broader NAND industry has had limited exposure to the AI and accelerated computing industry until now, eSSDs have emerged as a memory solution that combines the speed, reliability, and scalability needed for AI and accelerated computing, while other NAND-based storage options simply can't keep up with the demands of these workloads. Of note, eSSD shipments rose 86% Y/Y in 2024, a level last surpassed back in 2012, and expect it to grow HSD%/low-teens on average over the next 3 years as AI infrastructure growth continues at an unabated pace.

AI inferencing structural demand implications to storage

As the datacenter buildout continues at an unabated pace, CSPs are shifting focus from AI training to AI inference. While DRAM was a major beneficiary of training workloads, mainly driven by GPUs requiring high bandwidth memory (HBM), storage (HDD/SSD) had a limited role to play in the training dataset loading stage. However, as we transition to inference workloads, NAND becomes structurally more important as retrieving and analyzing data from trained models to generate responses demands very fast read speeds and minimal latency. In addition to this, while the initial AI model training requires massive datasets, the inferencing stage also needs quick access to significant amounts of data, making the high performance of SSDs necessary.

Going back to the initial days of AI when Chatgpt was introduced in Nov 2022, AI models were small and could easily fit in standard memory and storage. When Chatgpt was initially launched, it was likely using a GPT-3.5 model with a size ranging from tens of GBs (for smaller versions) up to ~350 GB (for the largest version), depending on deployment and optimization. However, as the number of parameters rises and as the world moves towards multimodal AI models, storage needs are expected to rise to tens of TBs per model.

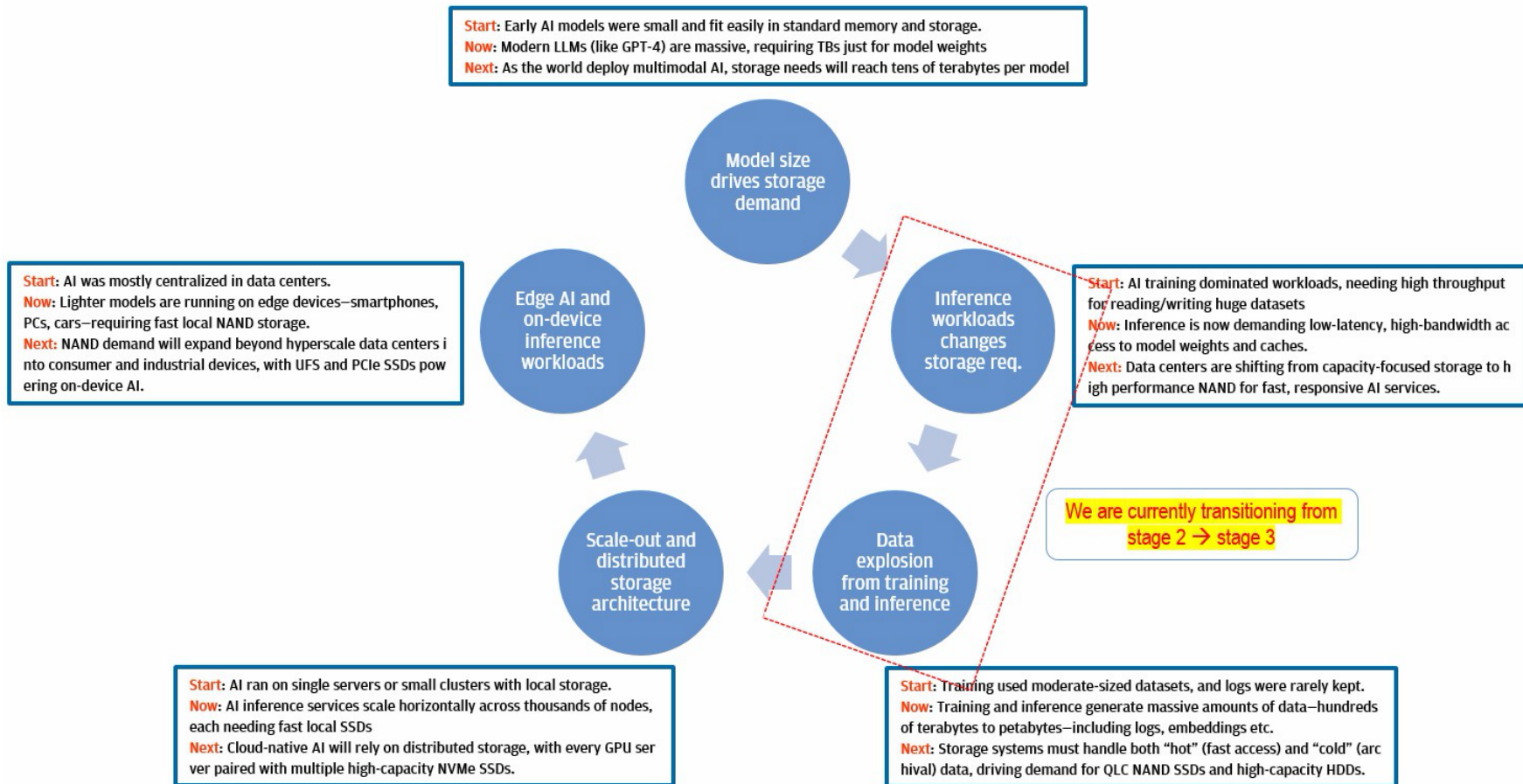
It is important to note that while AI training workloads require high throughput to run multiple operations on massive datasets, inference applications require low latency and high bandwidth access to model weights and caches, which is driving demand for higher capacity SSDs. In addition, commentary from NAND makers' CY2Q25 earnings calls highlights that CSPs are shifting their focus from pure capacity-based storage to high performance-based storage, which delivers an amalgamation of performance, power efficiency and density.

As consumers rapidly adopt multi-modal models into their daily workflows, both training and inference will generate massive amounts of data which needs to be stored for multiple purposes, such as log maintenance, embeddings, etc. While early storage systems were mainly required for cold data, moving forward, storage systems must be capable of handling both "hot" (fast access) and "cold" (archival) data, which is driving massive demand for QLC NAND SSDs and high-capacity HDDs. As per Trendforce ([link](#)), soaring inference AI demand is triggering severe nearline HDD shortages, which could potentially drive additional demand for QLC SSD shipments in 2026.

Moving forward, we expect that cloud-native AI will rely on distributed storage, with each GPU server paired with multiple high-capacity NVMe SSDs, and as AI models transition from datacenters to on-device, we expect NAND demand to expand into consumer and industrial devices, with UFS and PCIe SSDs powering on-device AI.

Of note, when a NAND maker mentions "NAND Flash driven by an NVMe-based controller that communicates over a PCIe connection", they essentially mean the NVMe-based controller manages and secures communication between the NAND flash and the CPU/system memory while the PCIe connection is the physical and logical pathway that allows the NVMe controller (and thus the NAND flash) to communicate quickly with the CPU and other components. (check Tables 2 & 3 below for more detail). Both storage controller protocols and higher-speed interfaces play an important role in enabling inferencing applications at the most optimized pace possible.

Figure 38: Evolution of AI storage needs



Source: Company reports and J.P. Morgan estimates.

Table 1: Storage characteristics comparison between SSD and HDD required for inference workloads

Characteristic	SSD	HDD
Random small-IO IOPS	10 ⁴ -> 10 ⁶ + IOPS	~50-200 IOPS
Latency	tens-hundreds micro secs	~5-15 milli secs
Sequential throughput	high	good for large sequential reads
\$/GB	higher	lower
Endurance	limited but improving	long lifetime for sequential writes
Best fit for inference	Hot data	cold/archival, backups

Source: Micron & Kioxia technical notes.

Table 2: Storage controller protocols

Rank	Protocol/Controller	Typical Max Speed*	Typical Use	Notes
1	NVMe (Non-Volatile Memory Express)	Up to 14 GB/s (PCIe Gen5 x4)	High-end SSDs, data centers, enterprise, consumer PCs	Fastest; designed for flash storage over PCIe
2	UFS (Universal Flash Storage)	Up to 4 GB/s (UFS 4.0)	Smartphones, tablets	Fastest in mobile/embedded; still slower than NVMe
3	SAS (Serial Attached SCSI)	Up to 2.4 GB/s (SAS-4)	Servers, enterprise storage	High speed, robust, used in enterprise
4	SATA (Serial ATA)	Up to 0.6 GB/s (SATA III)	Consumer SSDs, HDDs, legacy systems	Widely used, but slower than SAS/UFS
5	AHCI (Advanced Host Controller Interface)	Up to 0.6 GB/s (SATA III)	Older SSDs, HDDs	Protocol for SATA, not optimized for SSDs
6	eMMC (embedded MultiMediaCard)	Up to 0.4 GB/s (eMMC 5.1)	Budget smartphones, IoT, embedded	Lowest speed, used in cost-sensitive devices

Source: J.P. Morgan.

Table 3: High-speed interfaces for connecting storage

Rank	Interface	Typical Max Speed*	Typical Use	Notes
1	PCIe (Peripheral Component Interconnect Express)	Up to 64 GB/s (PCIe Gen5 x16)	Storage, graphics cards, network cards, SSDs	Fastest; used for internal high-speed connections
2	Thunderbolt	Up to 40 Gb/s (Thunderbolt 3/4) ~ 5 GB/s	Laptops, external SSDs, docking stations	Uses PCIe and DisplayPort protocols; fastest for external devices
3	SAS (Serial Attached SCSI)	Up to 24 Gb/s (SAS-4) ~ 2.4 GB/s	Servers, data centers	High speed, robust, enterprise storage
4	UFS Interface (Universal Flash Storage)	Up to 4 GB/s (UFS 4.0)	Smartphones, tablets	Fastest in mobile/embedded; not used for PCs
5	SATA (Serial ATA)	Up to 6 Gb/s (SATA III) ~ 0.6 GB/s	SSDs, HDDs, optical drives	Widely used, but much slower than PCIe/Thunderbolt
6	USB (Universal Serial Bus)	Up to 20 Gb/s (USB 3.2 Gen2x2) ~ 2.5 GB/s	External drives, flash drives	General-purpose, but slower than PCIe/Thunderbolt for storage
7	Ethernet/iSCSI	Up to 100 Gb/s (12.5 GB/s) for high-end Ethernet	NAS, SAN, enterprise environments	High theoretical speed, but real-world performance is often lower due to overhead/latency

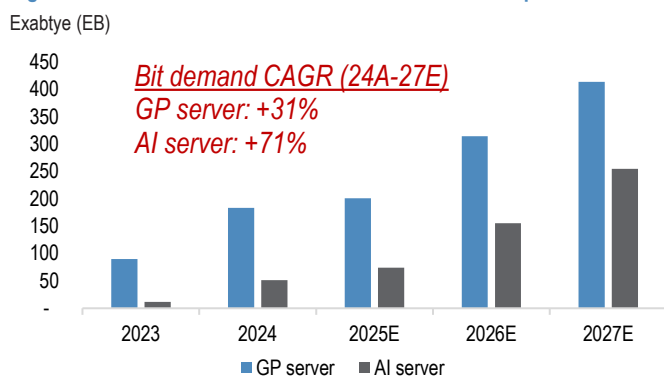
Source: J.P. Morgan.

KVcache offloading and HDD shortage driving eSSD demand

Once a function of storage demand only, we believe the value of eSSD is evolving not only to be a critical component to power Agentic AI for real-time data generation, but also for optimizing the model efficiency. During CES 2026, NVDA claimed that its Inference Context Memory Storage (ICMS) Platform utilizing BlueField-4 DPU delivers additional context storage at a 5x higher tokens-per-second and 5x more power efficient than traditional storage ([link](#)). Offloading KVcache to storage from GPU/HBM has long been the thesis of eSSD dem and growth but we believe the adoption of blue-field 4 DPU could potentially scale the accessible external storage, driving incremental SSD demand.

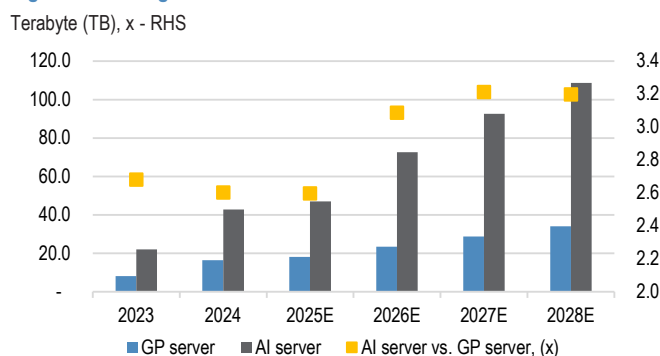
Based on our estimates, we expect the storage content/server gap between AI and GP server to widen to 3-3.2x given the need to store warm data for fast and real-time token generation. We expect this will trigger 50%+ content growth for AI servers, necessitating each AI server to carry at least 70+TB of storage with likely higher storage content in future years. Similar to DRAM, we believe the bulk of the NAND bit demand growth in 26-27E should be driven by servers amid consumer-exposed client SSDs (i.e. mobile/PC applications) likely showing weakness from BOM cost pressure-driven ASP hikes. We expect eSSD to account for 48% of the total NAND bit demand in 27E growing from 29% contribution in 25E.

Figure 39: eSSD GP server vs AI server bit demand comparison



Source: IDC, Gartner®, J.P. Morgan estimates.

Figure 40: Storage content difference between GP vs AI server



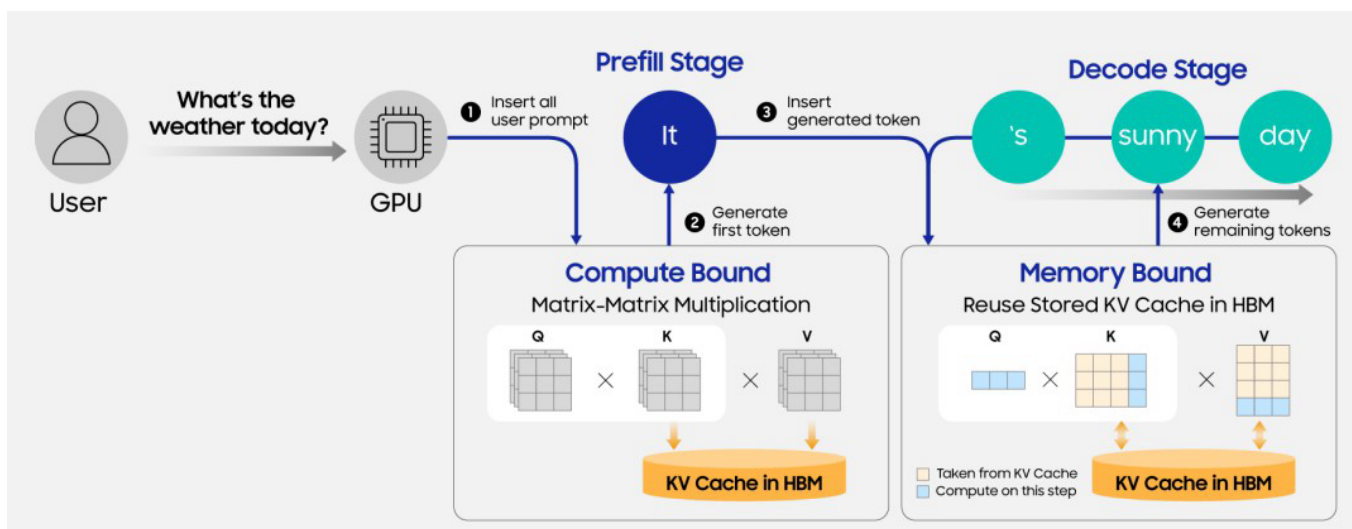
Source: Gartner®, J.P. Morgan estimates.

What is KVcache and why is it important?

As the number of tokens that need to be generated is becoming larger and faster (= lengthening context length), GPU memory limitations are becoming a critical bottleneck, making KVCache offloading an essential method for scaling inferencing workloads. Inferencing flow is broadly divided into two steps: 1) Prefill stage (input or understanding the prompt) and 2) the decode stage (output or the number of token generation). The KV Cache plays a critical role in optimizing decoding performance – particularly for long-context workloads and realtime generation scenarios – by enabling efficient reuse of previously computed representations.

- **Prefill stage:** In the prefill stage, the full prompt (Q) is processed once to generate the initial set of key-value pairs, which are stored in high-bandwidth memory (HBM) as the KV Cache. This stage is compute-bound, dominated by matrix–matrix operations, and it produces the first output token while initializing the cache for subsequent decoding.
- **Decode stage:** In the decoding stage, the model uses the stored KV cache together with the most recently generated token to produce the next token. Only the key-value pair for the new token is computed and appended. Because decoding proceeds token by token, it requires less compute per step but involves frequent HBM access, making it primarily memory-bound.

Figure 41: LLM Inference Flow with KV Cache



Source: Samsung Electronics.

NVDA Blue-field 4 DPU impact on the NAND industry

In CES 2026, NVDA introduced the Inference Context Memory Storage (ICMS) platform powered by BlueField-4 DPU (Data Processing Unit) which helps deliver additional context storage at a 5x higher token-per-second and 5x more power efficient than traditional storage ([link](#)). Since there is a KV cache limitation on GPU/HBM, the DPU allows GPU/HBM to access a remote storage at low latency, accelerating the computation speed and the pressure on GPU/HBM. Based on NVDA spec-sheet, the DGX SuperPOD is equipped with BlueField-4 carrying 512GB storage ([link](#)) with access to 600TB fast storage ([link](#)). Since Rubin GPU-based DGX SuperPOD is not the mainstream product, we expect the overall implications to NAND demand to be limited at this point. Nonetheless, we believe the structural trend remains intact, with SSD playing a critical role in AI computation process with upside to storage content per AI server rack.

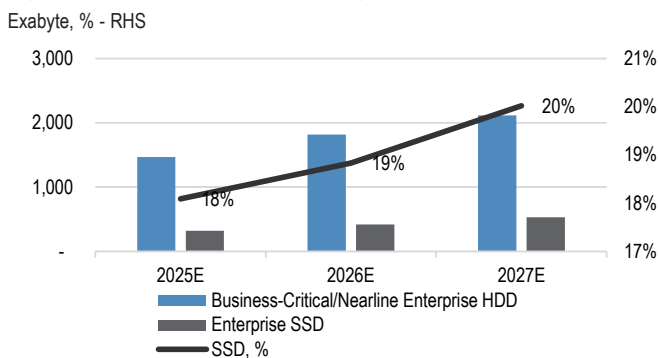
SSD vs HDD TAM analysis

Since 3Q25, the eSSD market has gained attention as a beneficiary of AI inferencing applications (necessitating high-performance read/write SSD to feed real-time data) and potentially replacing NR HDD for warm/cold storage function due to the long lead-time (max 2Y). Based on Gartner® data, Business-critical NR storage segment is still an under-penetrated segment with SSD accounting for 19% of total bit demand in FY26E (NR HDD bit demand was ~1800EB vs SSD ~420EB). This contrasts to the mission-critical SSD segment, where SSD shares already reached mid-90%. Within the business-critical NR storage segment, the economics of SSD vs HDD are not intuitive given SSD's 7-8x ASP premium over HDD, but we believe single-digit % SSD BOM cost share in AI server rack is forcing CSP's to adopt SSD over HDD due to performance and leadtime advantages. Since HDD makers (i.e. STX/WDC, etc.) have guided for a cautious capex outlook in CY26E, we expect eSSD to enjoy the demand tailwind in the next 12M causing a significant NAND price hike (JPMe: NAND industry ASP rising by 40% in FY26E). Based on the current 18-19% penetration rate, we highlight that an incremental 1%pct SSD penetration will result in an additional US\$2M eSSD revenue, which equates to ~2% of NAND TAM in FY26E.

Over the last 10 years, SSD has gradually replaced HDD due to its advantages in product performance (i.e., faster read/write speed, less power consumption, form factor, etc.). We believe the replacement has occurred mostly in mission-critical applications (storage that requires high-performance read/write speed and typically stores hot data) vs business-critical/nearline applications (warm/cold data storage).

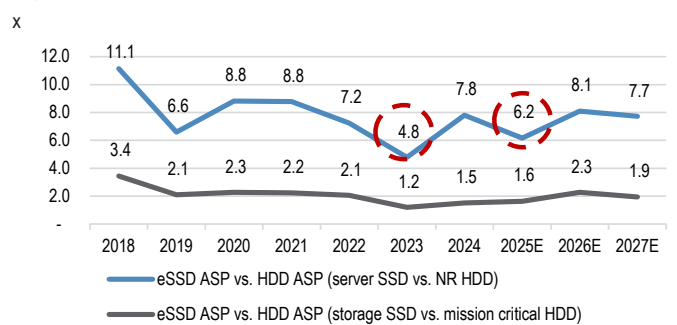
Interestingly, WD highlighted during its Investor Day that hard drives, again, will be the predominant storage media with over 80% of bits stored on hard drives. Seagate also highlighted on its recent earnings call highlighted that Hard drives continue to store close to 90% of the bits in large-scale data center deployments. We believe this shows *both HDD and SSDs are likely to complement each other*, with SSDs handling speed-sensitive tasks and HDDs providing affordable, large-scale storage.

Figure 42: Business critical vs server-grade SSD (EB)



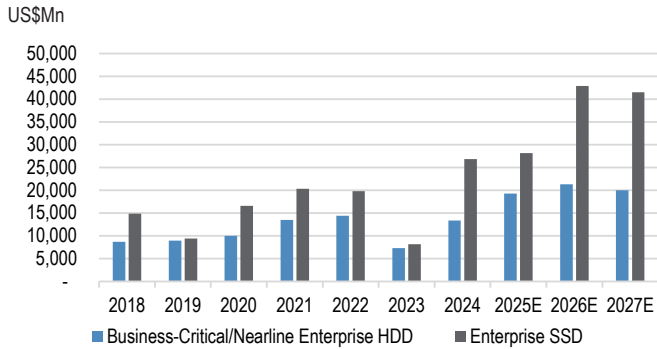
Source: Gartner®

Figure 43: eSSD ASP vs HDD ASP



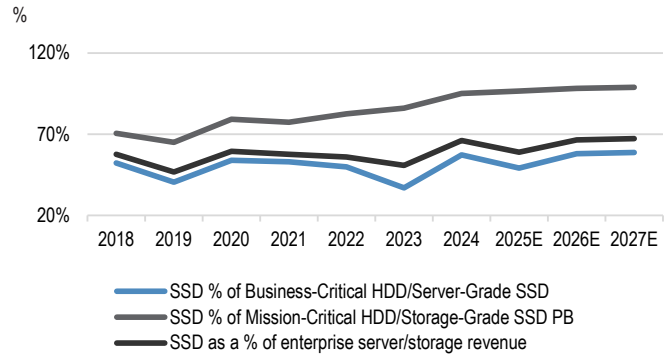
Source: Gartner®

Figure 44: Business critical NR HDD vs. SSD TAM comparison



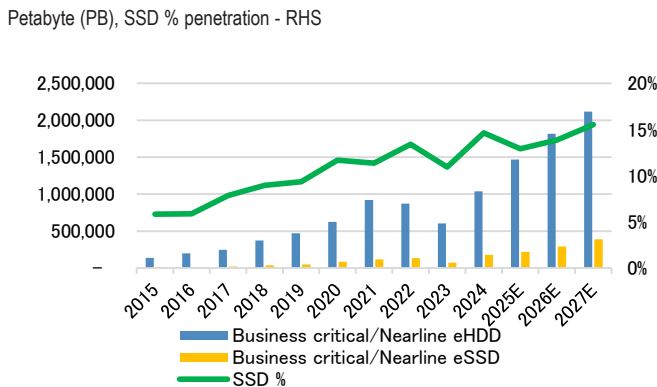
Source: Gartner®

Figure 45: SSD as a % of enterprise HDD TAM



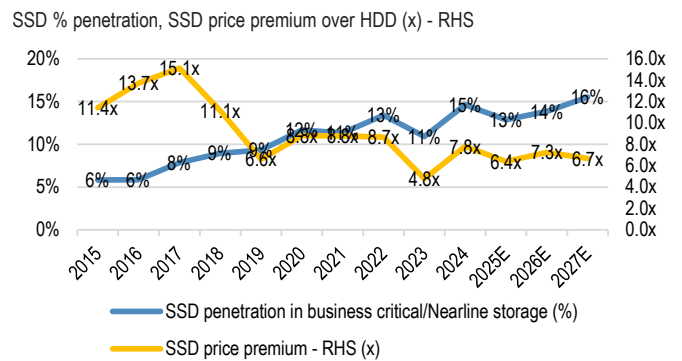
Source: Gartner®

Figure 46: Business-critical/nearline HDD and SSD shipment trends



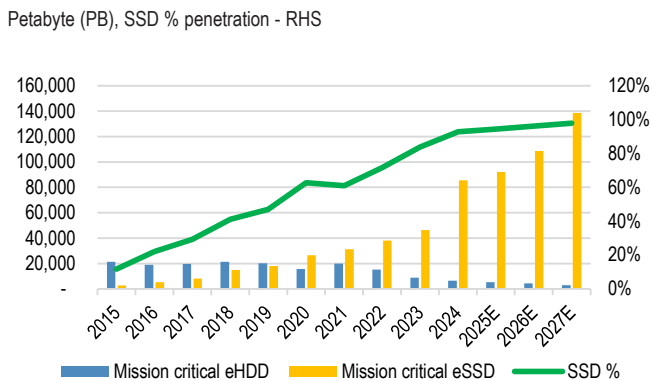
Source: Gartner®

Figure 47: SSD penetration in business-critical storage and SSD price premium over HDD



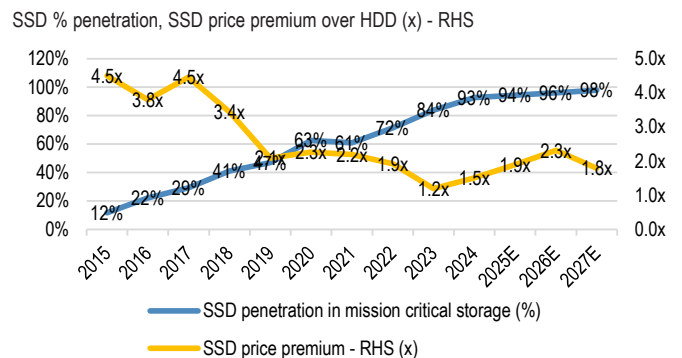
Source: Gartner®

Figure 48: Mission-critical HDD and SSD shipment trends



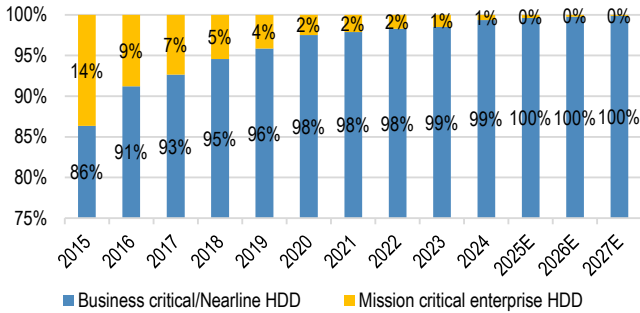
Source: Gartner®

Figure 49: SSD penetration in mission-critical storage and SSD price premium trend



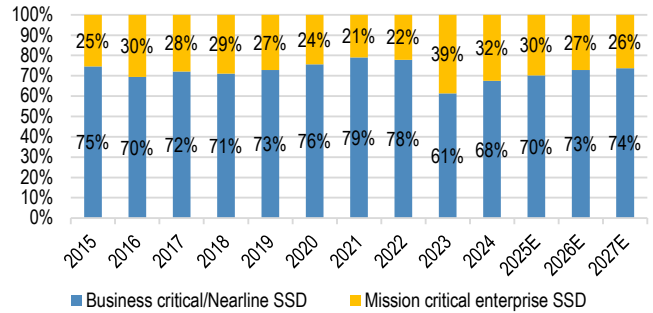
Source: Gartner®

Figure 50: Enterprise-grade HDD shipment mix



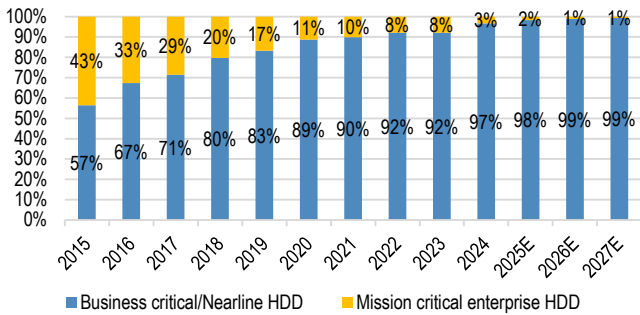
Source: Gartner®. Note: Shipments in PB.

Figure 51: Enterprise-grade SSD shipment mix



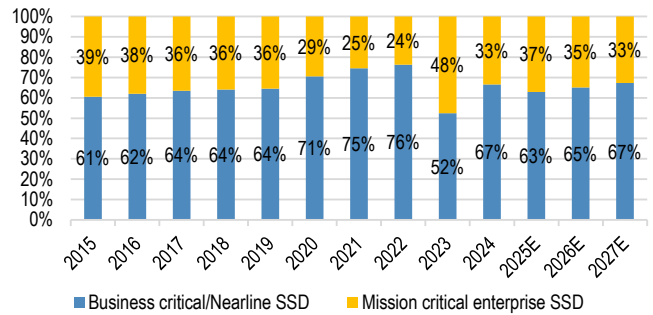
Source: Gartner®. Note: Shipments in PB.

Figure 52: Enterprise-grade HDD revenue mix



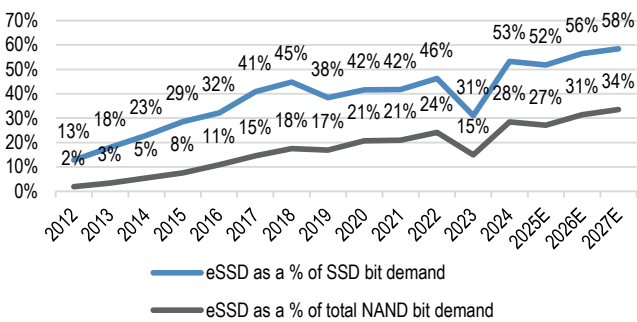
Source: Gartner®.

Figure 53: Enterprise-grade SSD revenue mix



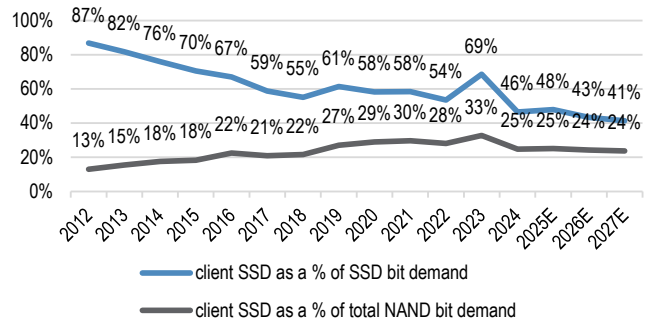
Source: Gartner®.

Figure 54: eSSD bit contribution in SSD and total NAND



Source: IDC, J.P. Morgan estimates.

Figure 55: Client SSD bit contribution in SSD and total NAND



Source: IDC, J.P. Morgan estimates.

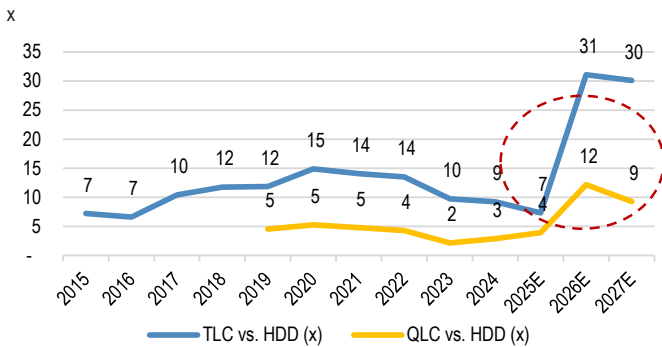
SSD vs HDD economics comparison

NAND flash makers have aggressively developed technologies to lower cost/bit via node migration and introduced QLC SSD in 2019, which theoretically carries ~33% higher bit/cell than TLC SSD via storing 4 bits per cell (vs 3 bits per cell in TLC). Lower price merits for QLC SSDs come at the expense of lower read/write speeds and endurance (vs previous product generations, such as SLC/MLC/TLC), but ensures much higher storage capacity and an alternative for datacenter storage devices, in our view.

When comparing blended NAND flash ASP by technology vs business-critical/nearline HDD ASP, we find that QLC ASP declined meaningfully until 2024, however, given the new demand tailwind for eSSD from KVcache offloading and HDD shortage, the price gap with HDD is expected to rise over the next 3 years, while other product generations trade much higher than HDD.

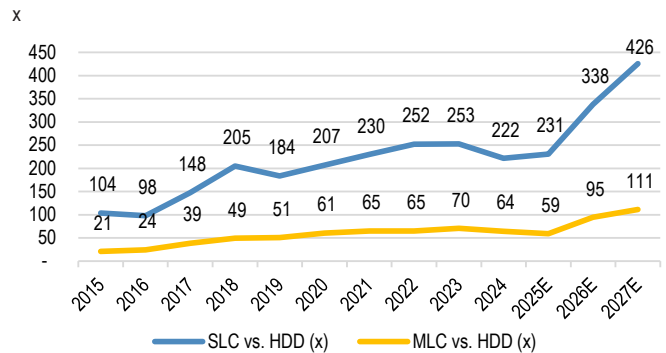
Nevertheless, we believe the reduced price gap between SSDs and HDDs, and heightened energy cost/heat dissipation focus in high-end AI servers, could continue to drive explosive demand for eSSDs due to its unique value proposition in the NAND market.

Figure 56: QLC/TLC ASP comparison vs. business-critical HDD



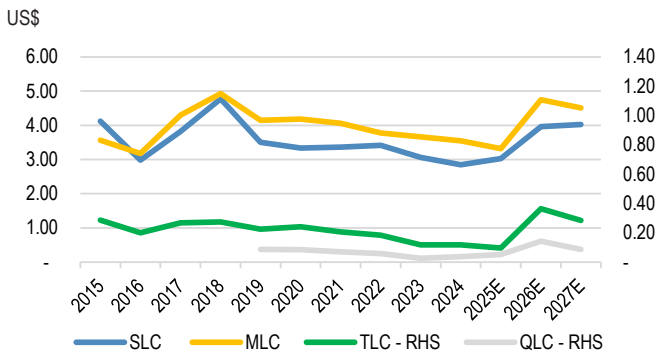
Source: Gartner®, OMDIA. Note: Blended QLC/TLC ASP (US\$, 8Gb equiv.) vs business-critical HDD price.

Figure 57: SLC/MLC ASP comparison vs. business-critical HDD



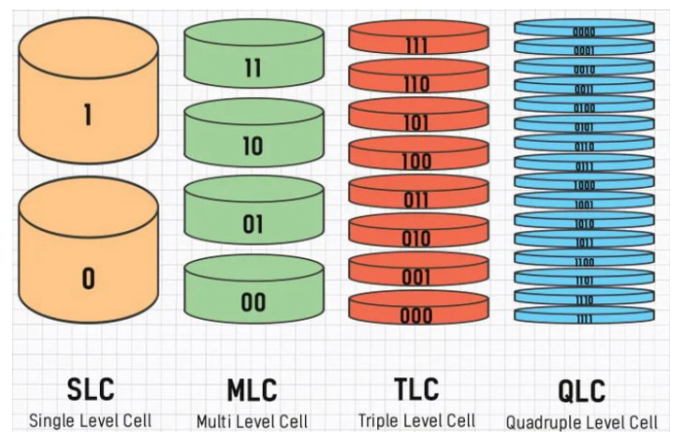
Source: Gartner®, OMDIA. Note: Blended SLC/MLC ASP (US\$, 8Gb equiv.) vs business-critical HDD price.

Figure 58: Flash ASP by technology



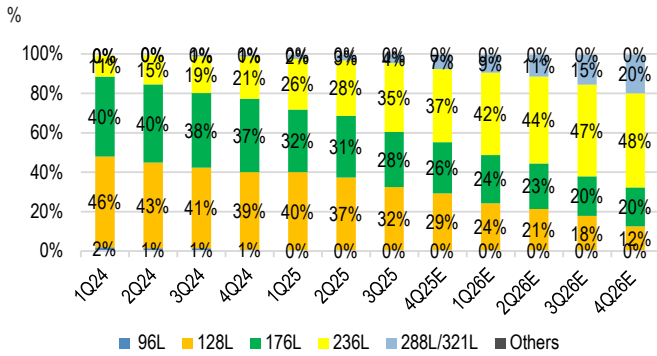
Source: OMDIA.

Figure 59: NAND Flash product by technology overview



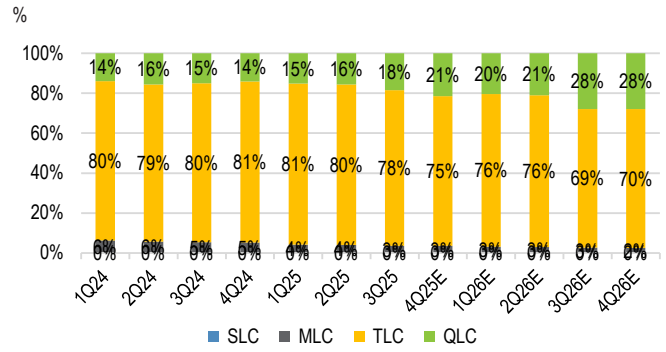
Source: SK hynix.

Figure 60: NAND bit production by layer count



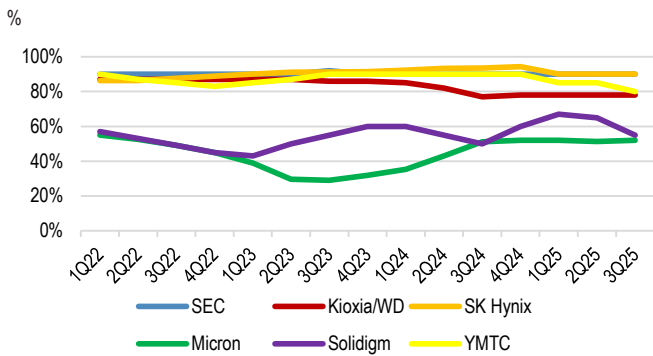
Source: OMDIA.

Figure 61: NAND bit share by technology



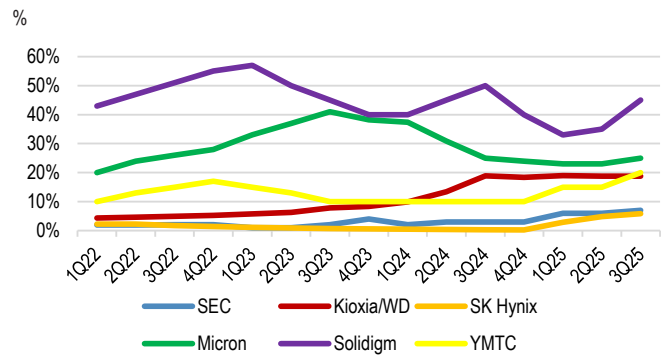
Source: OMDIA.

Figure 62: TLC shipment share by NAND makers



Source: OMDIA.

Figure 63: QLC shipment share by NAND makers



Source: OMDIA.

eSSD business comparison by major NAND suppliers

Among memory makers (assuming NAND exposure only), SKH has the highest exposure to the server mix, mainly driven by Solidigm’s leadership in the QLC space, followed by Kioxia and Samsung Electronics. However, when we compare the total server mix (both DRAM and NAND combined) between diversified memory makers (SEC, SKH and Micron) and pure play NAND makers (Kioxia), we observe that diversified memory makers continue to dominate the server space due to their exposure to the HBM market. However, going forward, we expect eSSDs to grow significantly due to their ability to combine the speed, reliability, and scalability needed for AI and accelerated computing.

For example, Kioxia’s server sales mix is currently below that of the diversified memory makers (see Table 4 below); we expect the mass production ramp of BiCS 8 to drive earnings expansion, positioning Kioxia for the strongest growth in NAND, followed by Samsung Electronics due to its product competitiveness in both TLC and QLC NAND. Samsung continues to lead the global market for **TLC NAND**, maintaining its position as the largest supplier by total bit volume and is currently mass-producing its **9th-generation V-NAND (V9)** using TLC technology, featuring a double-stack structure.

Table 4: Server sales mix comparison by memory makers

	2023	2024	2025E	2026E	2027E	25E-27E chg
SEC	29%	46%	53%	59%	66%	13%
SKH	49%	67%	69%	67%	76%	7%
Kioxia	20%	31%	34%	49%	61%	27%
Micron	n/a	n/a	56%	59%	60%	4%

Source: J.P. Morgan estimates, Company data. Note: Server sales include both DRAM and NAND for SEC, SKH, and Micron. Micron mix is based on new disclosures and future projections based on Bloomberg consensus.

- Solidigm (D5-P5336) is widely considered the leader in the high-capacity nearline segment, while SK Hynix excels in performance-driven workloads by leveraging their industry-leading layer counts (321L).
- Micron's 6500 ION eSSD is a strong competitor as well, though it uses "high-density TLC" (232-layer) instead of QLC to achieve similar 30.72TB capacities with better write endurance than traditional QLC.
- For performance-driven environments (AI, real-time analytics, and databases), Samsung (PM1743) and Kioxia (CM7-V)) hold the edge in raw speed and latency.
- Hence, Solidigm excels at QLC eSSDs, Samsung and Kioxia excel at TLC eSSDs, while Micron/SK Hynix are strong competitors as well. Of note, SKH targets to accelerate technology migration (300+L NAND bit mix target to reach 50%+ by 26-end) while for Micron, technology transitions to G9 will be the primary driver of their NAND bit growth in calendar 2026, and they expect it to become their largest NAND node in fiscal 2026.

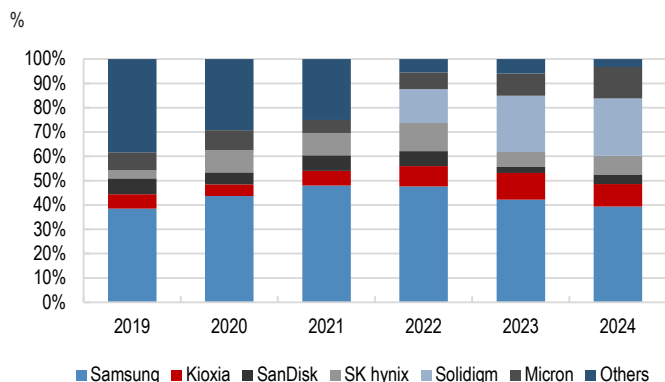
Table 5: Mainstream enterprise SSDs by NAND makers

Supplier	Mainstream Performance (TLC)	High-Capacity/Nearline (QLC)	Key Spec Highlights
Solidigm	D7-PS1010	D5-P5336/D5-P5430	PCIe 5.0 performance (D7); industry-leading 30.72TB & 61.44TB capacities (D5)
Samsung	PM1743/PM9D3a	BM1743 (V9 QLC)	PM1743 reaches 14 GB/s read speeds. V9 QLC production delayed to H1 2026.
Micron	9550/7450 PRO	6500 ION (DC QLC)	6500 ION uses high-layer TLC (232L) to compete with QLC in density but with better endurance.
Kioxia	CM7-R/CD8-R	G9 QLC	CM7-R uses BiCS TLC for 2700K IOPS random reads. New G9 QLC launched in Jan 2026.
SK Hynix	PS1010	321L QLC	PS1010 supports PCIe 5.0, up to 15.36TB. Sequential reads up to 14.8 GB/s, 321L QLC has a 2Tb die (world's first 300+ layer).

Source: J.P. Morgan estimates, Company data.

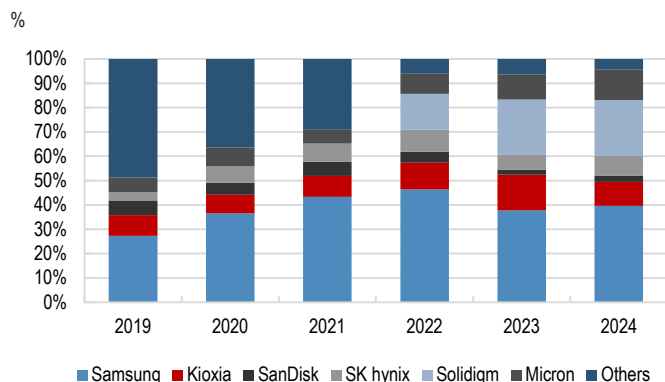
Historical Market share trends for eSSD

Figure 64: eSSD market share (GB basis)



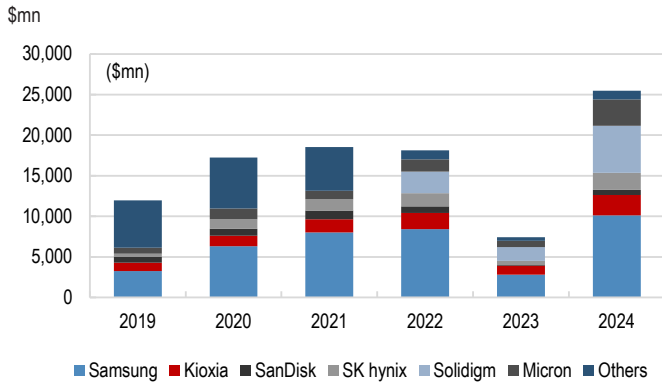
Source: OMDIA, J.P. Morgan estimates.

Figure 65: eSSD market share (value)



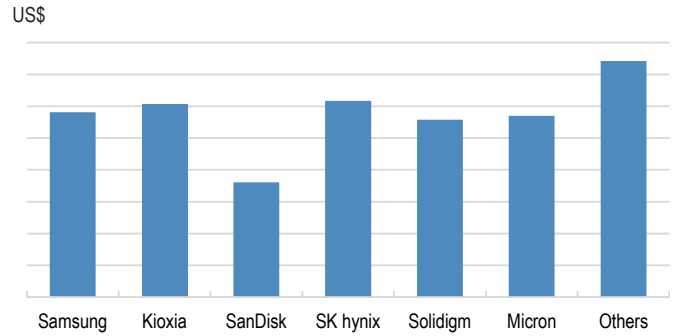
Source: OMDIA, J.P. Morgan estimates.

Figure 66: eSSD sales trend



Source: OMDIA, J.P. Morgan estimates.

Figure 67: eSSD ASP (2024)



Source: OMDIA, J.P. Morgan estimates.

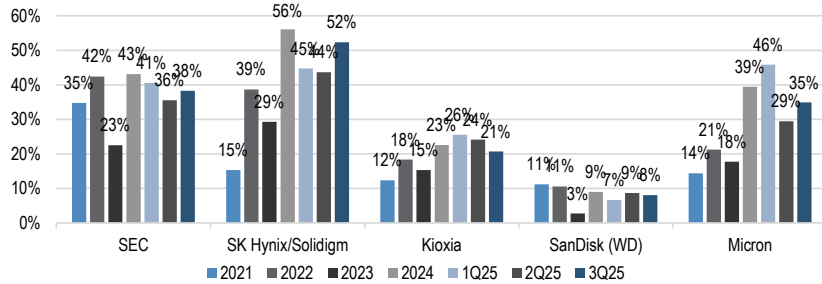
eSSD Business Comparison by Suppliers

eSSD sales exposure varies among NAND flash makers, with SK Hynix leading the charge with ~48% of its total NAND sales coming from eSSDs in 9M25, mainly driven by its exposure to this segment through its acquisition of Solidigm. It is followed by SEC and Micron, whose eSSDs contribute 36% each to their respective NAND sales, followed by Kioxia and SanDisk. Interestingly, the three NAND makers (SEC, SKH/ Solidigm and Micron) account for up to ~86% of the total eSSD market, which highlights the concentrated nature of eSSD sales.

Recent earnings calls from leading NAND makers show that strengthening eSSD demand is a key growth driver, strengthening NAND profitability even as suppliers reallocate resources towards more profitable AI products such as High Bandwidth Memory (HBM). Micron reported record revenue in its data center SSD business for fiscal 2025, supported by its technology leadership and vertical integration, while both Korean memory makers sounded extremely optimistic about eSSD sales during their latest 3Q25 earnings calls.

Of note, market analysis firm TrendForce is projecting a tightening of eSSD supply in 2026, with strong demand continuing through 2027, mainly driven by rapid advancements in AI, while nearline HDD supply is critically lagging demand, with extended lead times creating a substantial storage gap. As a result, data centers and CSPs are compelled to adopt high-capacity QLC enterprise SSDs to replace HDDs, which we believe will continue to drive demand for eSSD for leading NAND makers over the next 2 years.

Figure 68: eSSD sales exposure by NAND maker



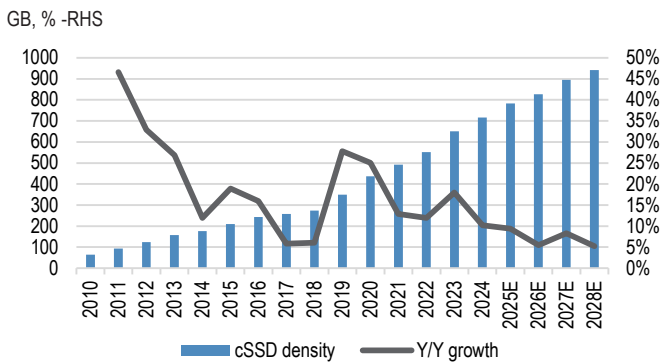
Source: Company data, OMDIA. Note: eSSD sales as a % of total NAND sales, WDC split into Seagate & WDC with Seagate getting the NAND/eSSD business while WDC getting the HDD business.

Consumer Electronics: Growth saturation in Mobile/PC market

Client SSD trend in PC market

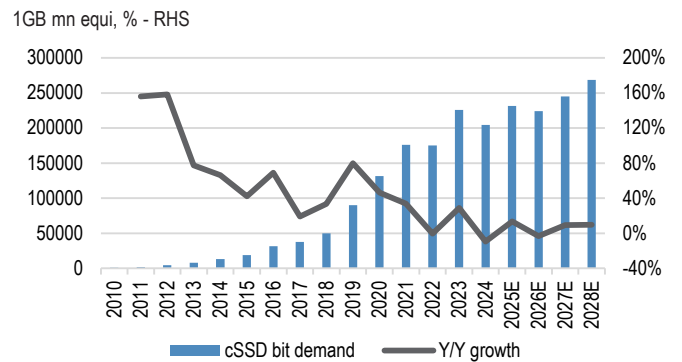
Following 3 years of negative system unit shipments, NBPC had a good year in 2025 with shipments rising HSD %, mainly driven by the emergence of AI PCs and Windows 10 EOL. While AI PCs are expected to pick up further in 2026, we believe cautious consumer spending amidst macro uncertainty, coupled with rising BOM costs (memory, components, etc.), will weigh on notebook brands' margins. If the unprecedented rise in memory prices continues unabated in 2026, we believe there is a high possibility that NBPC's end demand unit shipments will be revised downwards. Nonetheless, the transition to AI PCs will enable structural content growth, as many AI workloads rely on local models, vector databases, and larger application footprints. Hence, despite limited unit growth, we believe client SSDs will be driven by structural capacity growth.

Figure 69: cSSD LT content growth trend



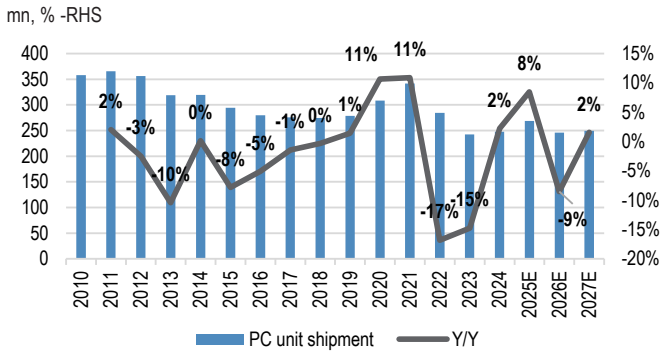
Source: IDC, Gartner®, J.P. Morgan estimates.

Figure 70: cSSD LT bit growth trend



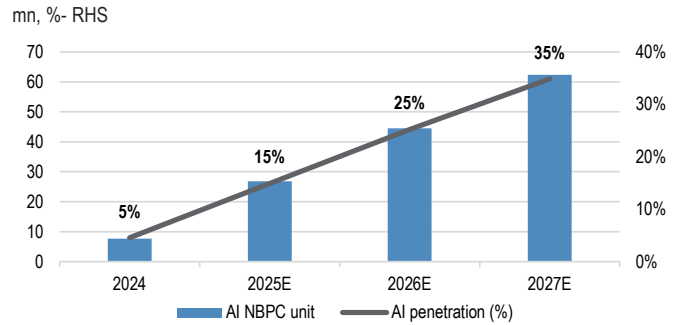
Source: IDC, Gartner®, J.P. Morgan estimates.

Figure 71: Total PC unit shipment trend



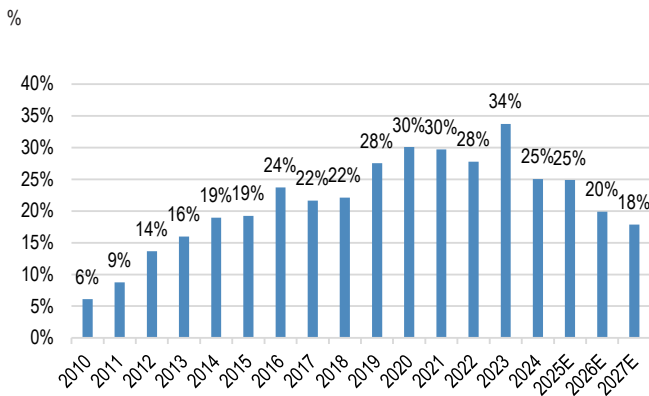
Source: IDC, Gartner®, J.P. Morgan estimates.

Figure 72: AI PC shipment and penetration trend



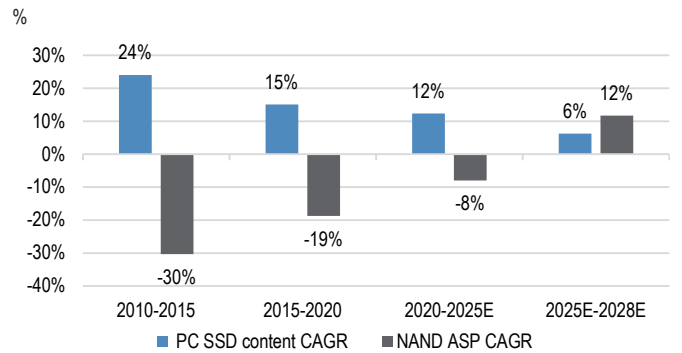
Source: IDC, Gartner®, J.P. Morgan estimates.

Figure 73: PC as % of total NAND demand



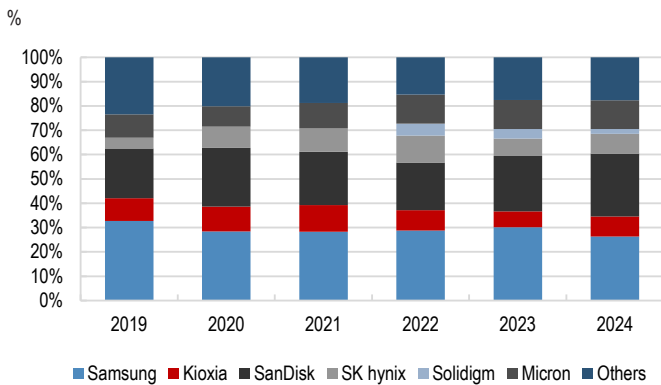
Source: IDC, Gartner®, J.P. Morgan estimates.

Figure 74: NBPC contents CAGR vs NAND industry ASP CAGR comparison



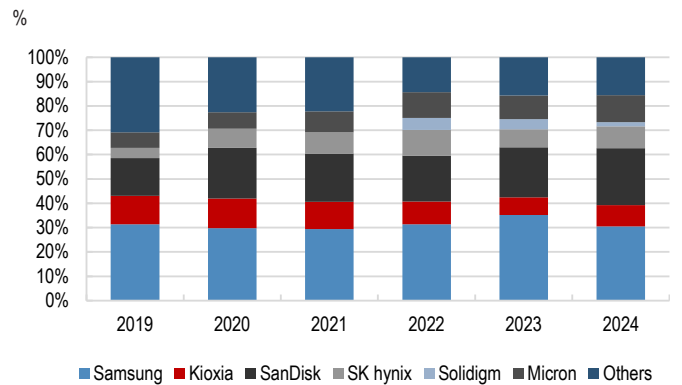
Source: IDC, Gartner®, J.P. Morgan estimates.

Figure 75: cSSD market share (GB basis)



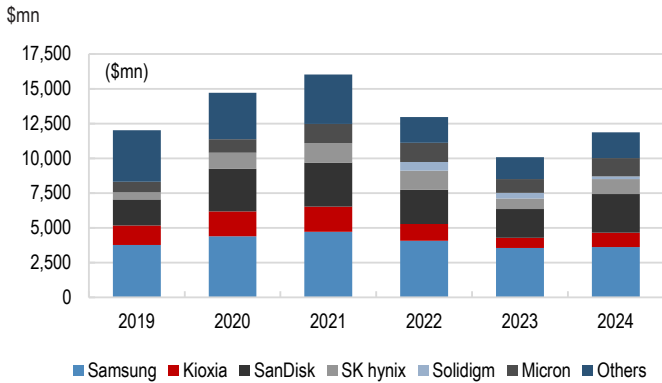
Source: OMDIA, J.P. Morgan estimates.

Figure 76: cSSD market share (value)



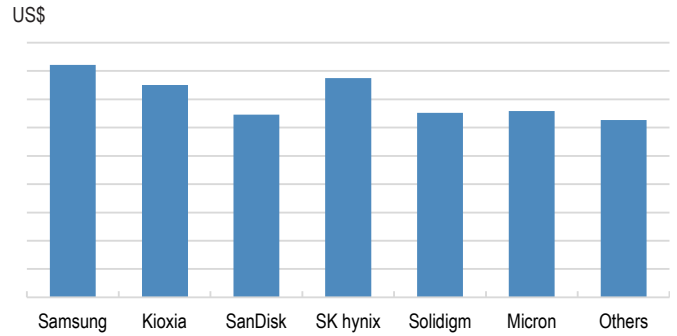
Source: OMDIA, J.P. Morgan estimates.

Figure 77: cSSD sales trend



Source: OMDIA, J.P. Morgan estimates.

Figure 78: cSSD ASP (2024)

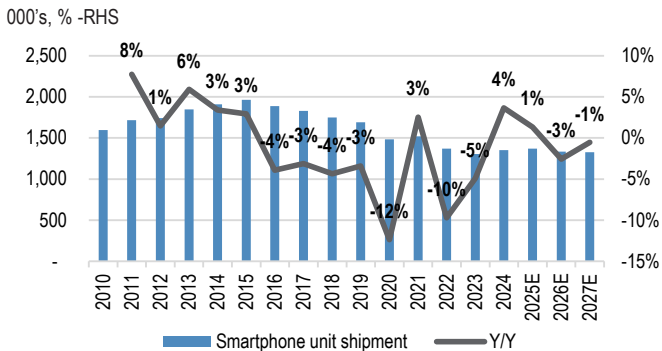


Source: OMDIA, J.P. Morgan estimates.

Demand Dynamics Update for Smartphones

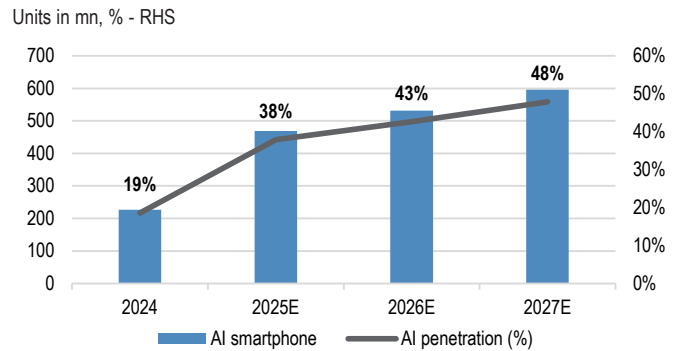
Following 2 years of positive unit shipment growth, global smartphone shipments are expected to shrink in 2026 as surging component costs are likely to impact demand. As memory prices continue to rise, BOM costs are severely impacting different tiers with the low end of the market (below \$200) being impacted most severely. To mitigate this impact, we expect OEMs to downgrade memory specifications (sticking with 128GB/256GB instead of 512GB/1TB) as price rises could further impact unit shipments.

Figure 79: Smartphone unit shipment trend



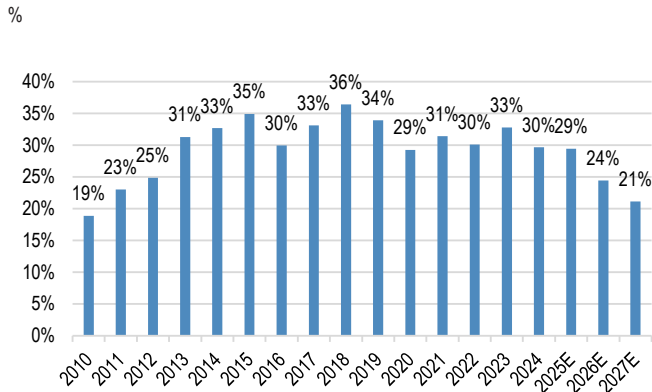
Source: IDC, Gartner®, J.P. Morgan estimates.

Figure 80: AI smartphone shipments and penetration



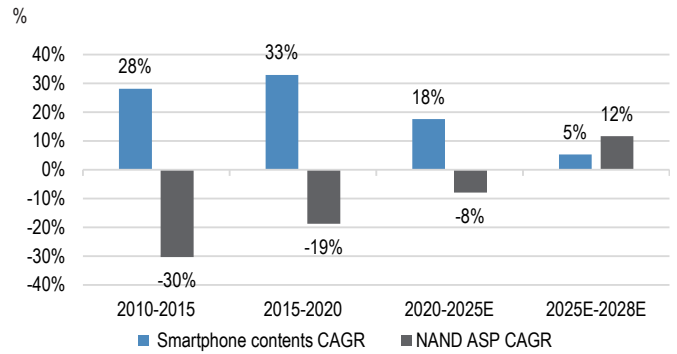
Source: IDC, Gartner®, J.P. Morgan estimates.

Figure 81: Smartphone as % of total NAND demand



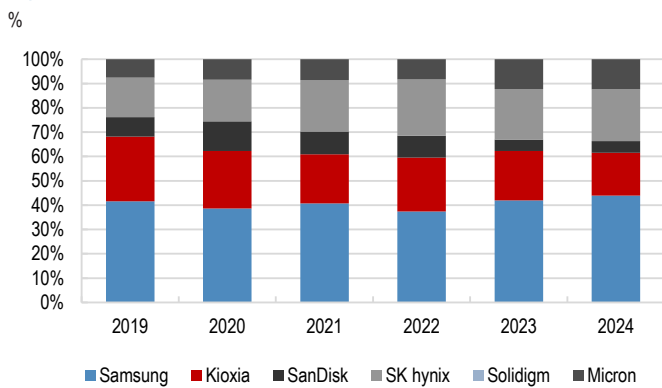
Source: IDC, Gartner®, J.P. Morgan estimates.

Figure 82: Smartphone contents CAGR vs NAND industry ASP CAGR comparison



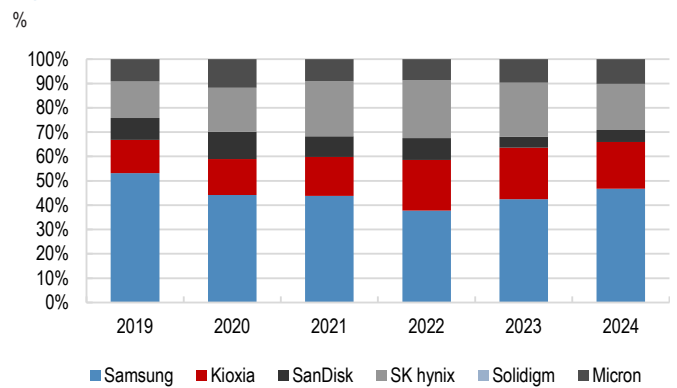
Source: IDC, Gartner®, J.P. Morgan estimates.

Figure 83: Smartphone NAND market share (GB basis)



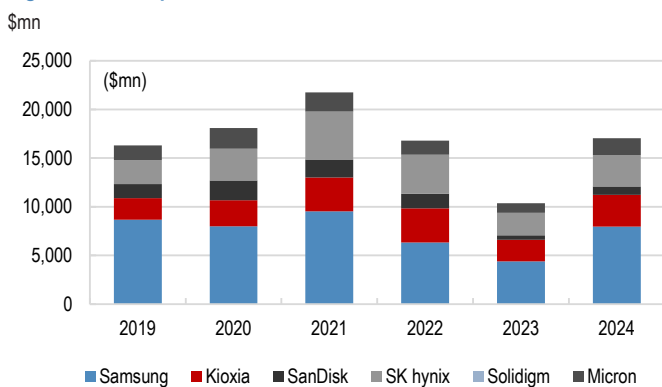
Source: OMDIA

Figure 84: Smartphone NAND market share (value)



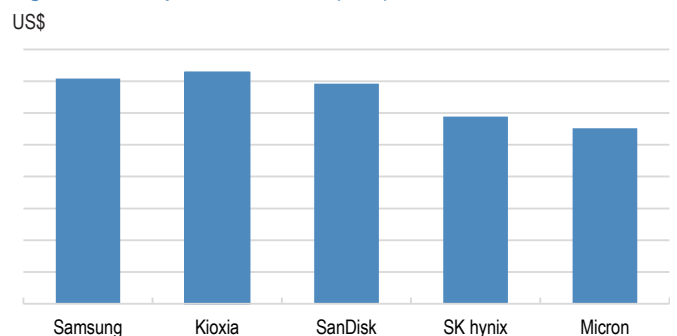
Source: OMDIA

Figure 85: Smartphone NAND sales trend



Source: OMDIA

Figure 86: Smartphone NAND ASP (2024)



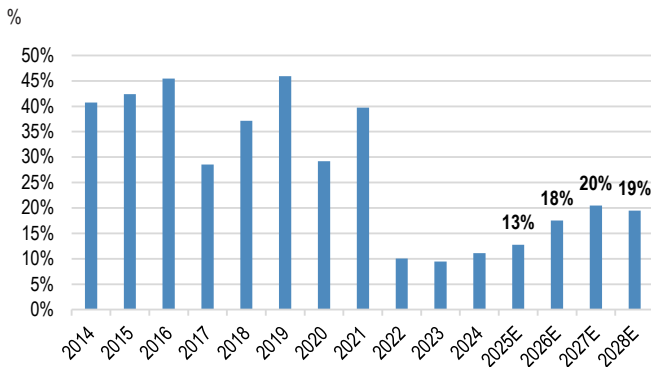
Source: OMDIA

NAND supply dynamics

NAND bit growth trend

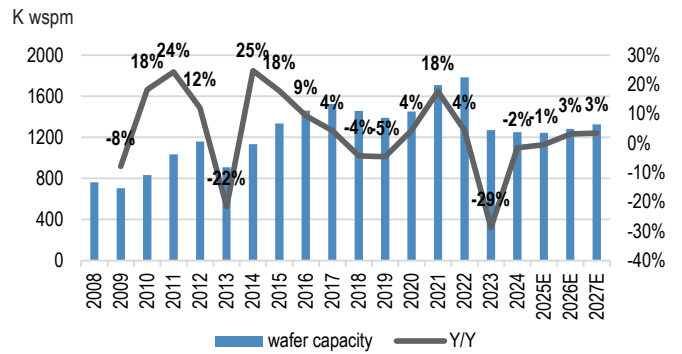
Following COVID-19, the NAND industry underwent an unprecedented downcycle in 2022-23, characterized by crashing prices, plummeting revenues, and negative profit margins for major manufacturers. The industry went through major inventory destocking, driven by weak demand for consumer electronics. As a result, NAND B/G plummeted to low-10% for the next 3 years from 2022-24 (NAND B/G in 2021: 40% Y/Y) as excess inventory went through a correction. As a result of this, major suppliers – Samsung, SK Hynix, Kioxia and Micron – responded by reducing production and slowing down technology migration in an attempt to stabilize the market. While NAND had a limited role to play during the AI training phase (compared to DRAM), the transition to inference workloads, coupled with HDD shortages, drove accelerated demand for eSSD. As a result, NAND supply bit growth (B/G) rose to mid-teens % in 2025. Going forward, given tight S/D dynamics coupled with limited capacity additions, we expect NAND B/G to be in the high-teens % range over the next 3 years.

Figure 87: NAND supply bit growth trend



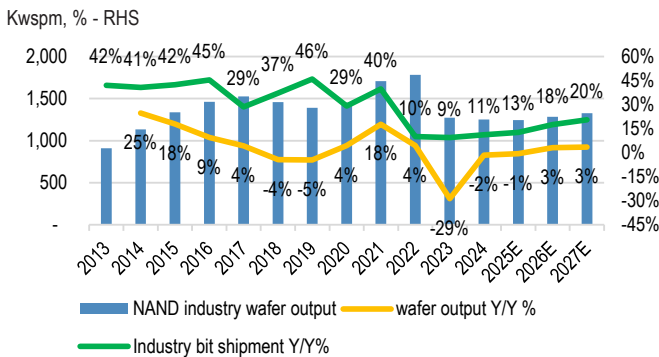
Source: WSTS, J.P. Morgan estimates.

Figure 88: NAND wafer output



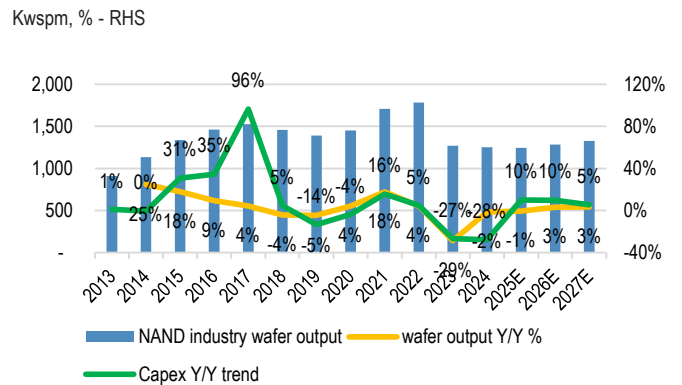
Source: J.P. Morgan estimates, Company data.

Figure 89: NAND wafer output vs industry bit shipment Y/Y growth trend



Source: J.P. Morgan estimates.

Figure 90: NAND wafer output vs NAND capex Y/Y growth trend



Source: J.P. Morgan estimates, Company data.

NAND bit production mix comparison

As of 2025, the majority of bits are still below 2xx layers despite the industry rapidly scaling past the 176-layer era, which is the mainstream standard. Leading manufacturers such as Samsung and SK hynix have established **236-layer** and **238-layer** architectures as their primary high-volume "workhorse" nodes, while mass production of **321-layer** (SK hynix) and **332-layer** (Kioxia/Western Digital) NAND has begun to meet the surging storage demands of AI data centers. When we compare the NAND makers' potential bit mix by layer composition for 2026, we expect that barring Kioxia and SKH, all other memory makers would make 2xx layers their major node, while SKH ramps its 321L further into year end '26.

Table 6: 2026E NAND bit production mix by layers by suppliers

%

Bit mix by layers	Kioxia+SNDK	SEC	SKH+Solidigm	YMTC	MU
<=192L	72%	28%	45%	15%	12%
192L> and <=286L	28%	72%	32%	85%	88%
286L>	0%	0%	23%	0%	0%
Total WSPM	402	390	203	165	125

Source: OMDIA. Note: Kioxia also preparing 332L (BiCS 10) from 2027E onwards in terms of layer migration competition. Note: YMTC (unlisted) is estimated by J.P. Morgan based on publicly available data.

Industry wafer capacity trends

When comparing the wafer capacity trend by location for NAND makers, we observe that barring Samsung and Micron, all other NAND makers are concentrated in a single location. We believe that given the geopolitical uncertainties, it's important for NAND makers to diversify their production bases across regions. However, the recent escalation by the United States through export controls designed to restrict China's ability to produce advanced semiconductors, including cutting-edge NAND flash memory, is affecting operations for SEC and SKH, which operate significant NAND fabs in China (Xi'an and Dalian/Wuxi, respectively). If we look at the last 13 years of global NAND wafer capacity mix by location, we observe that while South Korea and Japan occupied ~80% of the production base as of 2025, NAND makers have diversified their production bases with all 3 (South Korea, China and Japan) occupying an equal 30% share, respectively, a trend we believe is unlikely to persist as geopolitics put a damper on NAND makers' ability to expand before 200 layers.

Table 7: Individual NAND wafer capacity by location

%	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025E	2026E
Samsung													
South Korea	94%	83%	77%	78%	79%	76%	75%	71%	64%	63%	55%	56%	55%
China	6%	17%	23%	22%	21%	24%	25%	29%	36%	37%	45%	44%	45%
Kioxia													
Japan	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
Micron													
United States	50%	45%	43%	37%	21%	20%	22%	23%	25%	27%	23%	23%	24%
Singapore	50%	55%	57%	63%	79%	80%	78%	77%	75%	73%	77%	77%	76%
SK Hynix													
South Korea	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
Solidigm													
China	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	100%
YMTC													
China					100%	100%	100%	100%	100%	100%	100%	100%	100%

Source: OMDIA.

Table 8: Global NAND wafer capacity mix by location

%	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025E	2026E
South Korea	40%	38%	37%	37%	38%	38%	38%	38%	36%	34%	31%	30%	28%
Japan	38%	37%	38%	38%	39%	37%	36%	35%	34%	33%	31%	30%	31%
China	2%	5%	7%	9%	10%	13%	15%	17%	21%	24%	28%	30%	31%
Singapore	10%	11%	10%	10%	10%	10%	9%	8%	7%	7%	8%	8%	7%
United States	10%	9%	7%	6%	3%	3%	3%	2%	2%	3%	2%	2%	2%
Global NAND WSPM	1,158	1,341	1,477	1,536	1,454	1,360	1,451	1,739	1,782	1,316	1,291	1,296	1,284

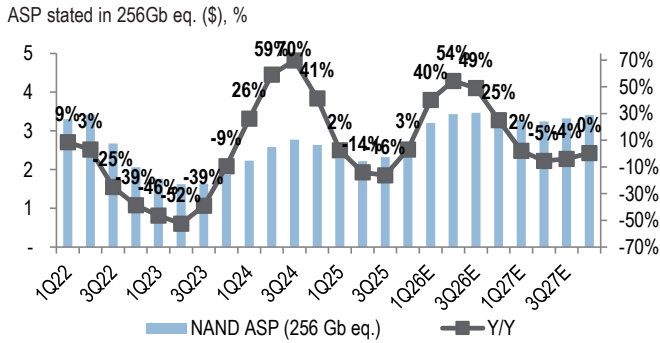
Source: OMDIA.

NAND ASP outlook

Spot price

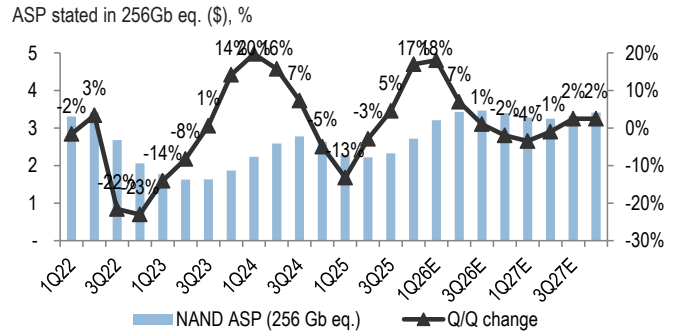
Spot prices for specific high-demand components, such as 512GB TLC wafers, have risen by 5.5x times over the past seven months, rising from approximately \$2.70 in July to ~\$15 in Jan 26. This dislocation between spot and contract prices suggests that “official” contract hikes are lagging behind the reality of physical scarcity. The shortage is most acute in the high-density segments utilized by enterprise clients (512Gb and 1Tb). Manufacturers appear to have adopted a strategy of gradually increasing contracted pricing, which should help to sustain upward momentum in pricing into 2026, though we do also anticipate a deceleration in ASP growth from 4Q26 and an eventual inflection lower heading into 2027 as industry supply-demand dynamics improve. We forecast blended ASP growth of +40%/-2% in 2026/2027.

Figure 91: NAND quarterly pricing trend and Y/Y trend



Source: WSTS, J.P. Morgan estimates.

Figure 92: NAND quarterly pricing trend and Q/Q trend



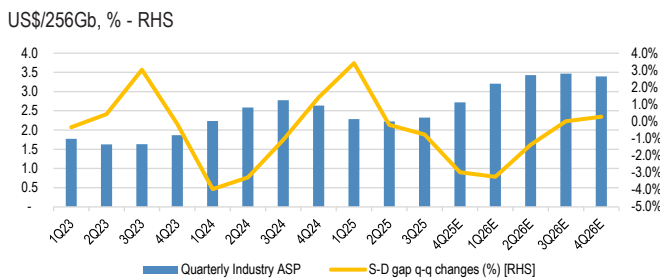
Source: WSTS, J.P. Morgan estimates.

NAND flash pricing momentum and operating profit leverage

Upward trend to continue throughout 2026, eSSD mix expansion to drive value growth in 2027

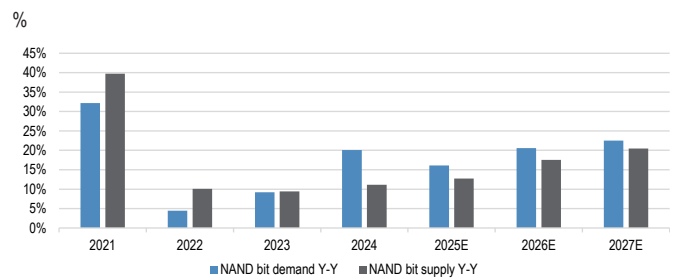
After a 20% cyclical price correction during 4Q24-2Q25, NAND pricing bottomed out in mid-2025, then started to rebound quickly due to strong enterprise SSD orders amidst only a gradual increase in supply (lead time to get NAND bits was 4-5 months and industry UTR was running at sub-80% for 6+months from 2H2024). Demand for high capacity SSD (QLC SSD for HDD replacement) and AI local storage grade SSD (TLC SSD for KV Cache) picked up, leading to sharp inventory digestion at memory maker/channel, resulting in spot prices rising 200-300% during September-December 2025.

Figure 93: Quarterly NAND industry ASP vs NAND industry S-D gap trend 1Q23-4Q26E



Source: WSTS, J.P. Morgan estimates.

Figure 94: NAND industry demand growth vs supply growth comparison 2021A-2027E



Source: WSTS, J.P. Morgan estimates.

The overall NAND ASP increase was relatively low (15-30%) in 4Q25A compared to compared to DRAM (rising 30-40%, depending on different grades/applications). However, we expect the price increase longevity to be similar to that of DRAM in the next 12-18 months thanks to the under-supply market conditions (2026E/2027E NAND demand +21%/+22% YoY vs supply +18%/+20%). We forecast 50-60% NAND contract ASP increase in the next four quarters (high-teens % in 4Q25, 20% +/- in 1Q26E, 10% +/- in 2Q26E, and low-to-mid single digit % in 3Q26E) supporting sharp margin recovery at NAND suppliers (industry operating profit margin advancing to high-30% this year from ~10% last year).

Based on our consumer end-demand disruption scenario (high BOM cost weighing on procurement sentiment and relatively high NAND channel inventory at end customers vs the DRAM channel), we expect diverging pricing momentum between B2B (Enterprise SSD) and B2C (Client SSD/Mobile and consumer electronics grade NAND) from the end of 2026E. However, as the eSSD grade NAND ASP premium over others expands (from +11% in FY2024A to +17%/+37% in FY2025E-2026E and higher in FY2027E), we believe rising eSSD volume mix will adequately offset any potential consumer NAND demand weakness. We expect NAND industry TAM to continue to grow well above double-digit % in 2027E, clearly setting a different cycle pattern from history (previously, upcycle durations were less than two years).

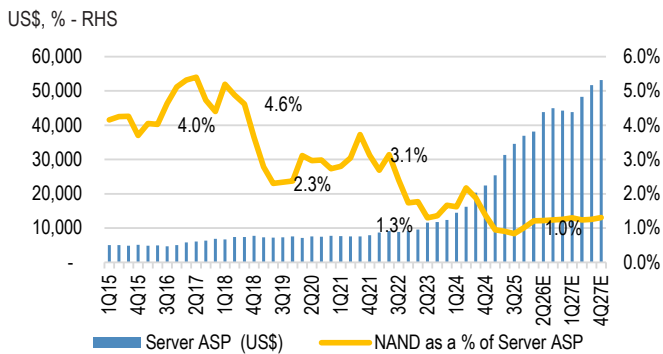
NAND value % contribution trend across end-applications

The chart below demonstrates historical NAND ASP as a % of device ASP across various end-applications to gauge the upside/downside room for NAND ASP hikes/cuts. As seen in Figures 95-100 below, while smartphone, NB and server ASPs have been on a gradual upward trend due to a shift to premium products and new form factors, NAND cost as a % of device ASP has been divergent between servers and NB/smartphones.

As for smartphones, we expect NAND ASP as a % of device ASP to rise to its highest level at 5.5% in 3Q26E driven by NAND ASP growth (vs 4.0% in 3Q18 during the 2016-18 server upcycle) and expect it to remain elevated for the next 2 years. In addition, NAND ASP as a % of device ASP has been on a structural downtrend for servers with NAND accounting for ~1% of the total ASP while being >5% during the 2016-18 server upcycle. Lastly, for NB, while it has been on a downtrend and reached as low as 4.3% during the unprecedented NAND downcycle, the ASP is expected to be >10% over the next 2 years, which highlights the rising BOM cost pressure for these CE OEMs.

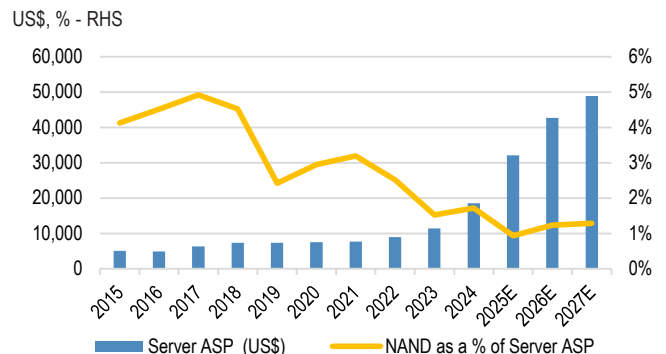
On a longer time horizon, as NAND bit demand growth slows, we believe the NAND industry will suffer from oversupply more frequently, as a result of which ASP will fall quickly, which will eventually drive either consolidation (Kioxia-WD) or capital discipline (SEC/cutting wafer starts) in the industry.

Figure 95: NAND cost as a % of server ASP



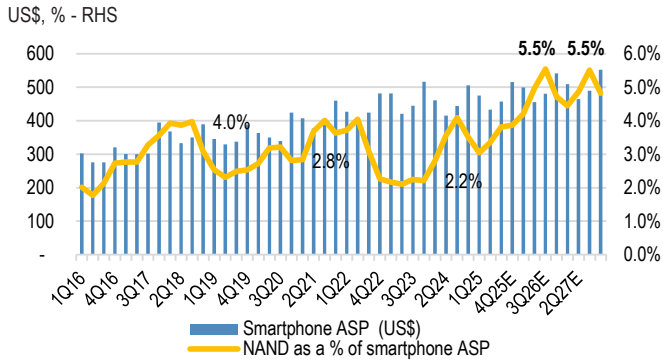
Source: IDC, J.P. Morgan estimates.

Figure 96: NAND cost as a % of server ASP



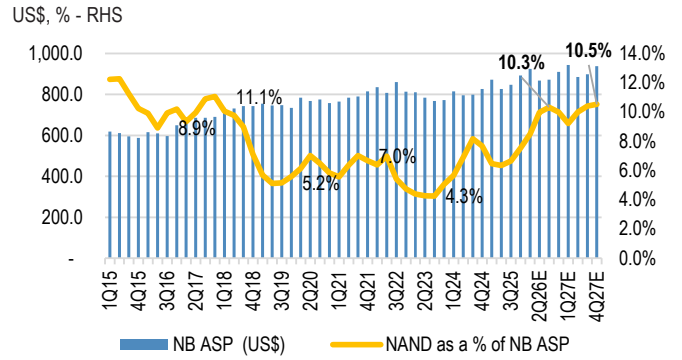
Source: IDC, J.P. Morgan estimates.

Figure 97: NAND cost as a % of smartphone ASP



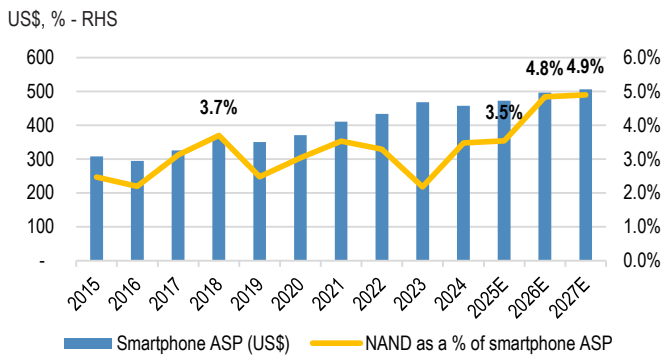
Source: OMDIA, J.P. Morgan estimates.

Figure 98: NAND cost as a % of NB ASP



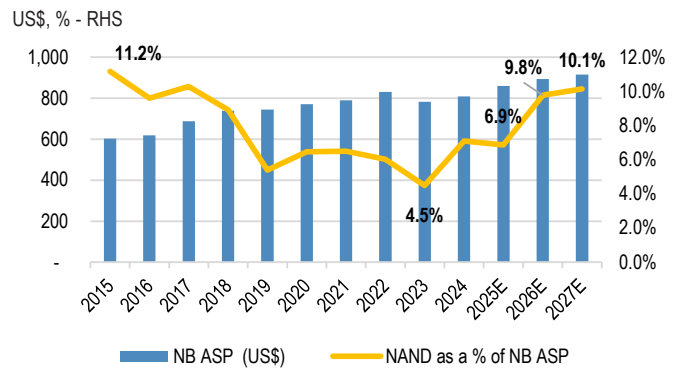
Source: IDC, J.P. Morgan estimates.

Figure 99: NAND cost as a % of smartphone ASP



Source: OMDIA, J.P. Morgan estimates.

Figure 100: NAND cost as a % of NB ASP



Source: IDC, J.P. Morgan estimates.

Peer Analysis

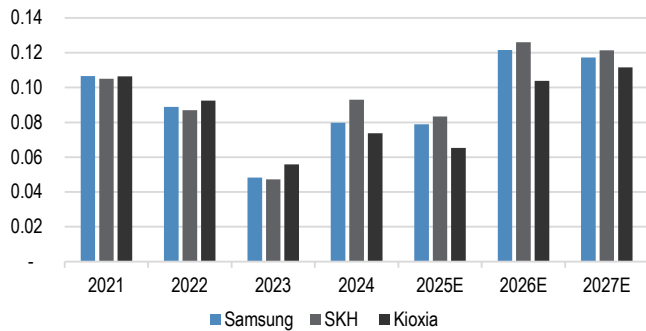
Key operating economics comparison

Stacking in NAND has undergone multiple technological innovations over the years, with NAND makers currently employing vertical scaling (>200 layers) as well as architectural scaling (such as CBA) that enables higher density and lower cost/bit. As NAND is a highly commoditized, capacity driven market, the most important economic driver in NAND flash is lower cost per bit as a better cost structure trumps limited pricing power.

It is important to note that demand for NAND is extremely price elastic, as evidenced by smartphones moving from 64GB to 128GB, etc., and SSD penetration replacing HDD as falling \$/GB makes high capacity economically viable. In addition, given the boom and bust nature of the NAND industry, ASPs could fall below cash cost (as evidenced during the 2022-23 downcycle) and only the lowest cost producers will survive in the long run. With NAND makers continuing to push the boundaries of innovation to meet the robust demand from AI applications, having an economically sound cost structure is imperative for long-term profitability and free cash flow generation.

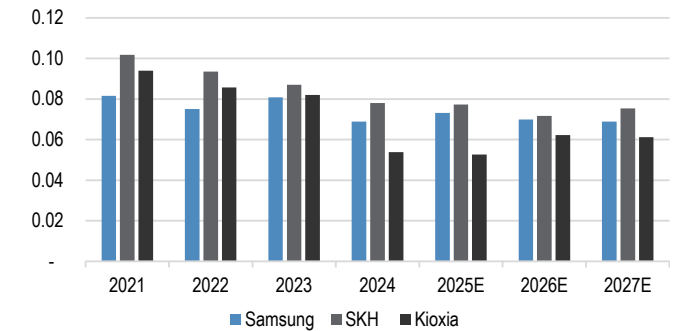
When we compare the top 3 NAND makers, Kioxia has demonstrated the lowest gross cost/bit economics vs peers, mainly driven by technological prowess (CBA) and more diversified product mix. As a result, despite not having the highest ASP/unit, Kioxia has had industry leading OP/bit economics over the last 3 years, which we believe is testament to their technological leadership in the NAND industry.

Figure 101: ASP/bit comparison between the leading 3 NAND makers
 US\$



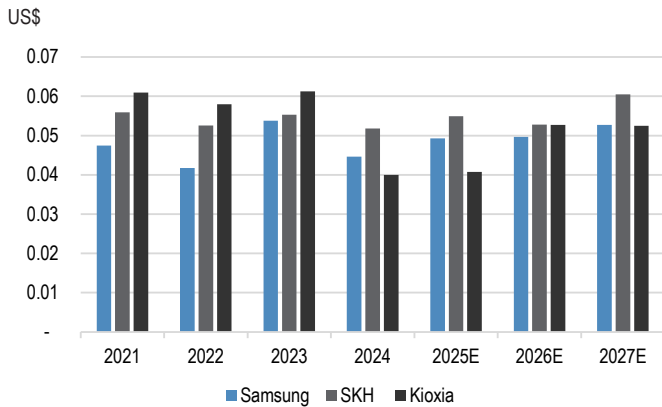
Source: J.P. Morgan estimates.

Figure 102: Gross Cost/bit comparison between the leading 3 NAND makers
 US\$



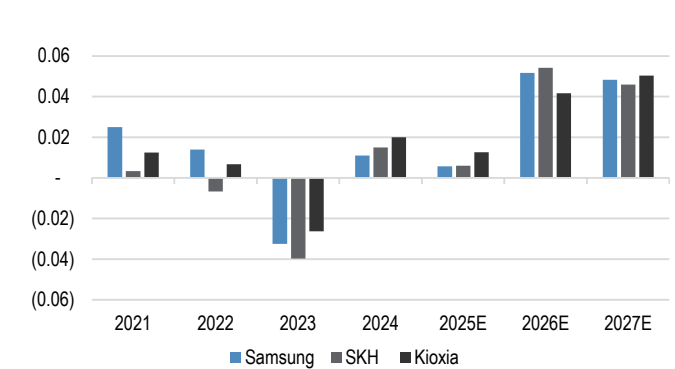
Source: J.P. Morgan estimates, Company data.

Figure 103: Gross cost less D&A/bit comparison between the leading 3 NAND makers
 US\$



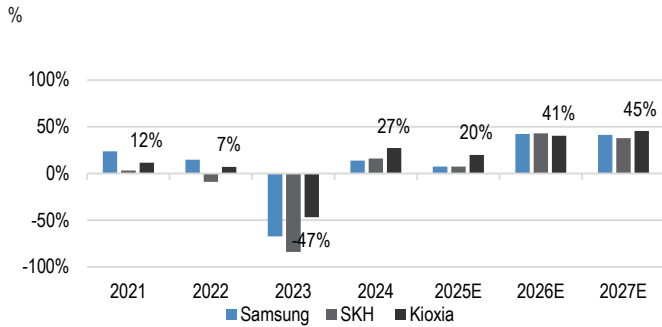
Source: J.P. Morgan estimates.

Figure 104: OP/bit comparison between the leading 3 NAND makers
 US\$



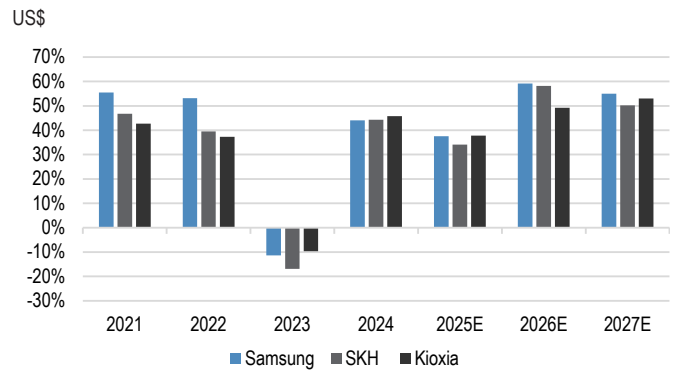
Source: J.P. Morgan estimates, Company data.

Figure 105: OPM comparison between the leading 3 NAND makers



Source: J.P. Morgan estimates.

Figure 106: EBITDA margin comparison between the leading 3 NAND makers

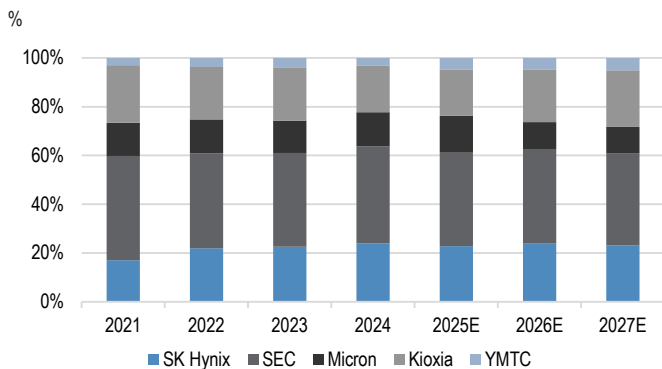


Source: J.P. Morgan estimates, Company data.

Competitive dynamics

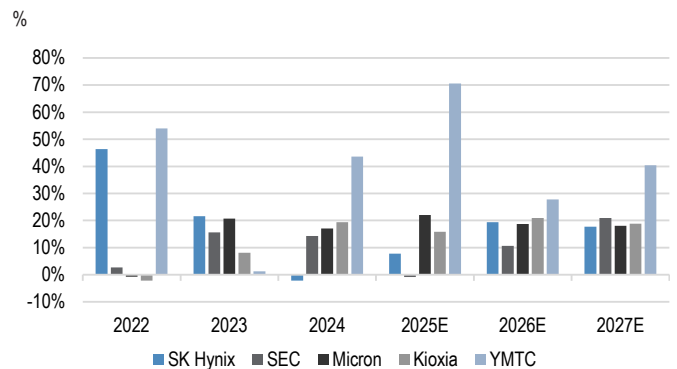
Samsung dominates the NAND market, maintaining the top position with an estimated mid-high 30% M/S, followed by Kioxia and SK Hynix. The top 3 players occupy ~80% of the total NAND market, with Micron and Yangtze Memory Technologies Corp (YMTC, not listed) occupying the rest, which highlights the oligopoly nature of the industry. A similar trend can be seen in wafer capacity M/S trends, however, despite having a greater share of wafer, YMTC occupies a smaller share of revenue due to lower yields vs peers. Given that NAND makers are focused on tech migration rather than greenfield capacity additions, we believe NAND B/G is expected to be in the high-teens % on average over the next 2 years.

Figure 107: Revenue M/S trend for NAND players



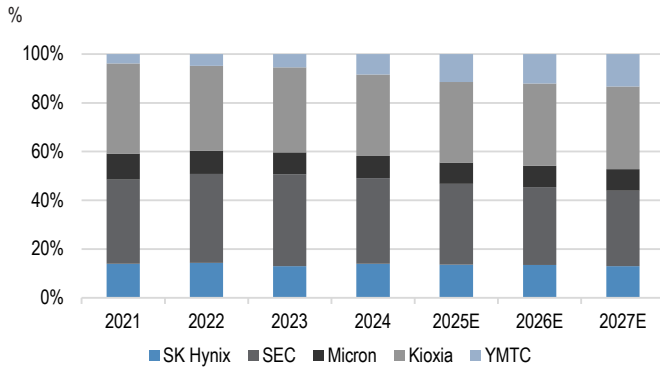
Source: J.P. Morgan estimates, Company data.

Figure 108: Y/Y B/G trend for NAND players



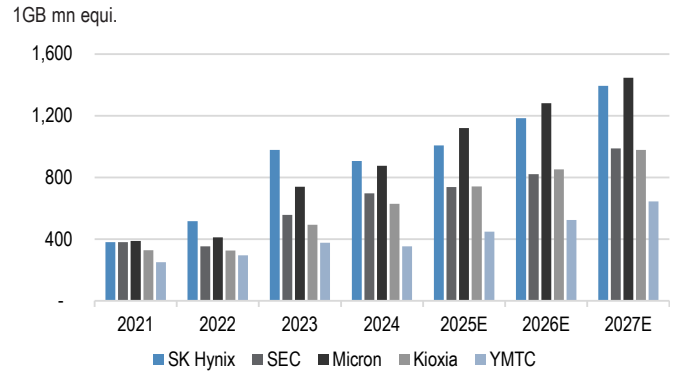
Source: J.P. Morgan estimates, Company data.
 Note: YMTC's (unlisted) next 3 years is estimated by J.P. Morgan based on publicly available data

Figure 109: Wafer capacity M/S trend for NAND players



Source: J.P. Morgan estimates, Company data.

Figure 110: Bit/capacity trend for NAND players



Source: J.P. Morgan estimates, Company data.

Technology Trends

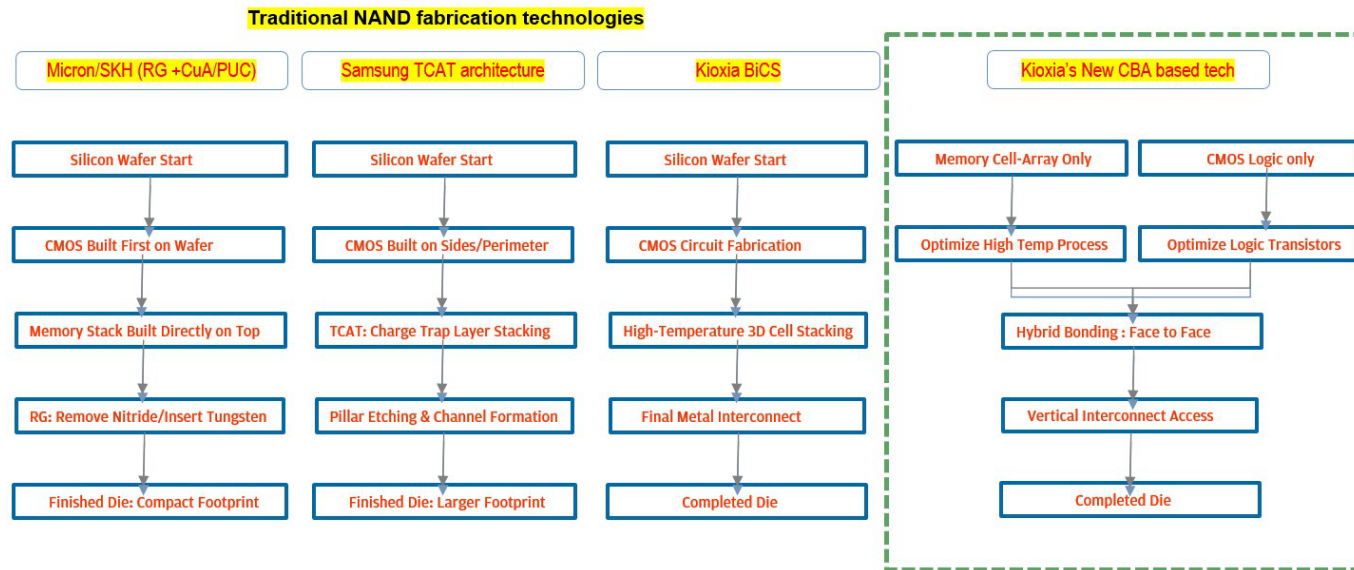
NAND memory manufacturing techniques

There are multiple technologies that are used in the development of NAND flash memory, but they differ in their approach and structure. Some of the leading technologies are as follows:

1. **Charge Trap Flash (CTF):** This technology uses a charge trap layer to store data, which can improve reliability and scalability compared to traditional floating gate flash memory. This method reduces cell-to-cell interference and allows for smaller cell sizes.
2. **Floating Gate NAND:** The traditional method for NAND flash memory, where data is stored in a floating gate transistor. This technology has been widely used for many years.
3. **Vertical NAND (V-NAND):** Developed by Samsung, V-NAND is a type of 3D NAND that stacks cells vertically, allowing for higher density and improved performance.
4. **BiCS (Bit Cost Scaling):** BiCS NAND is a type of 3D NAND technology developed by Toshiba (now Kioxia) that stacks memory cells vertically to increase storage density, which allows for more bits to be stored in the same footprint, improving cost efficiency and storage capacity.

With the ever-increasing need for storage in personal, professional, mobile and datacenter applications, there is little doubt that technology will continue to evolve in the future to meet market needs.

Figure 111: NAND fabrication technologies



CMOS integration: Kioxia uses **CBA** (CMOS Directly Bonded to Array), while peers use COP or CuA/PUC, meaning Kioxia directly bonds the CMOS circuitry to the memory array, which is a significant architectural revision.

Manufacturing: Kioxia employs a Dual-Wafer (Hybrid Bonding) process, whereas others use a Monolithic (Single Wafer) approach.

Gate Process: Kioxia's Gate-First/Last Hybrid is distinct from the Gate-Last (Replacement Gate) method used by peers.

Thermal Budget: Micron and Samsung (in PUC) build memory on top of logic; the high heat of memory fabrication can damage the logic below. Kioxia avoids this by building them separately.

Source: Company data.

NAND technology used in auto and consumer markets

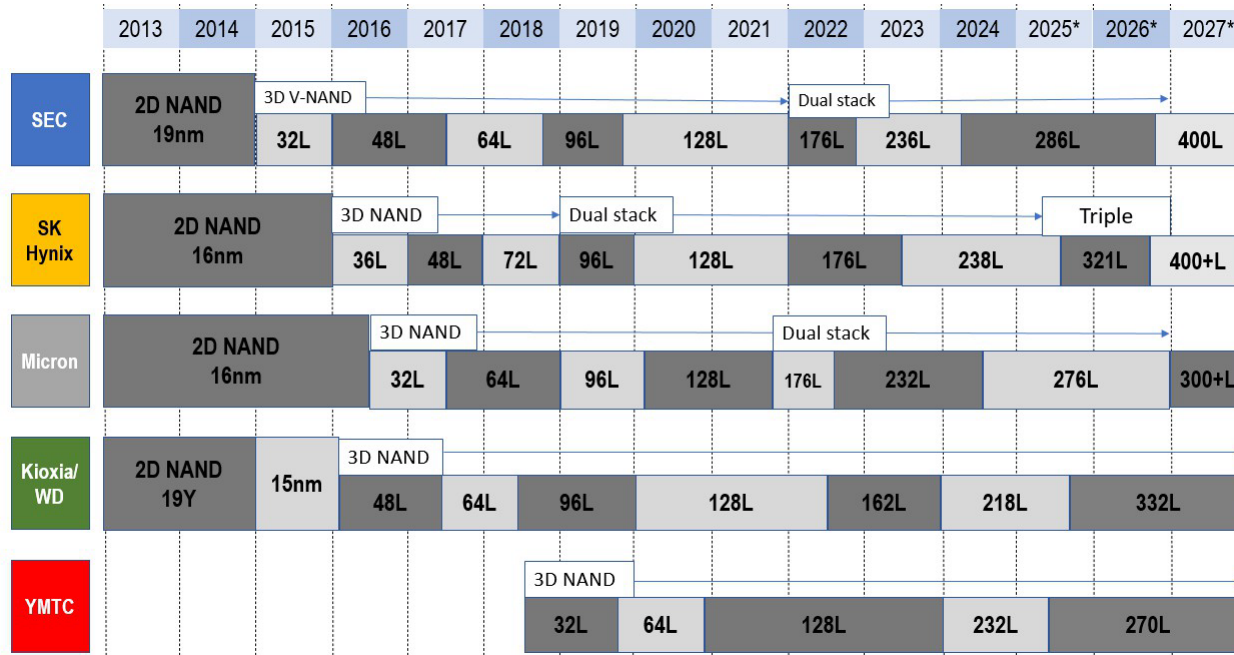
In modern vehicles, NAND flash memory is critical for a wide range of systems, from safety and diagnostics to entertainment. The NAND solutions used in automobiles, such as eMMC, UFS, and SSDs, are designed to endure extreme temperatures, vibrations, and high performance demands. Applications such as ADAS, autonomous driving, etc., rely on NAND memory to store and process real-time data from sensors, cameras and radars.

Table 9: Comparison between eMMC, NAND and UFS

	eMMC (embedded MultiMediaCard)	NAND (Raw NAND Flash)	UFS 4.1 (Universal Flash Storage)
Definition	Integrated storage solution with NAND flash and controller	Raw flash memory chip, requires external controller	Advanced storage solution with NAND and high-speed controller, designed for fast data transfer
Controller	Built-in controller manages ECC, wear leveling, bad block management	No controller; host system must manage all functions	Advanced built-in controller with improved ECC, wear leveling, and error management
Interface	Standardized (JEDEC/MMC), parallel interface	Custom, requires host-side management	Standardized (JEDEC/UFS), high-speed serial interface (MIPI M-PHY, UniPro)
Ease of Use	Plug-and-play, simplifies integration	Complex, requires firmware/software development	Plug-and-play, optimized for high performance and easy integration
Performance	Moderate, suitable for consumer devices	Can be optimized for high performance	Very high, supports fast read/write speeds, low latency, and high IOPS
Applications	Smartphones, tablets, consumer electronics, IoT devices	SSDs, enterprise storage, high-performance embedded systems	Premium smartphones, tablets, automotive, high-end consumer electronics
Capacity Range	Up to 256GB (some up to 512GB)	Wide range, from small to very large	Typically up to 1TB or more
Cost	Higher per GB due to integrated controller	Lower per GB, higher integration cost	Higher per GB, but justified by performance and features
Reliability	High, due to built-in management features	Depends on host controller/firmware	Very high, advanced error management and reliability features
Power Efficiency	Moderate	Depends on controller implementation	Excellent, optimized for mobile and battery-powered devices
Data Transfer Rate	Up to ~400 MB/s (eMMC 5.1)	Depends on controller and interface	Up to ~4,200 MB/s (UFS 4.1)

Source: Samsung blogs and flexxon.

Figure 112: NAND technology migration roadmap by memory maker



Source: Company data, J.P. Morgan estimates.

Table 10: 3D scaling technique in NAND

3D Scaling technique	Explanation	Technique	Leader
Lateral scaling	It involves increasing the density of memory cells horizontally across the chip	Achieved by reducing the size of each memory cell and optimizing the layout to minimize wasted space	Kioxia/SanDisk
Logical scaling	This involves the ability to store more bits per cell	Manufacturers can increase the overall capacity without increasing the physical size of the chip.	Kioxia/SanDisk
Vertical scaling	Vertical scaling involves stacking memory cells on top of each other	Multi-tiered memory holes and thin, low-resistive memory layers	Samsung
Architecture scaling	It involves changes in the overall design and structure of the memory chip	Techniques like CMOS Next to Array (CNA), CMOS Under Array (CUA), and CMOS Bonded Array (CBA) are used to optimize the architecture	Kioxia/SanDisk

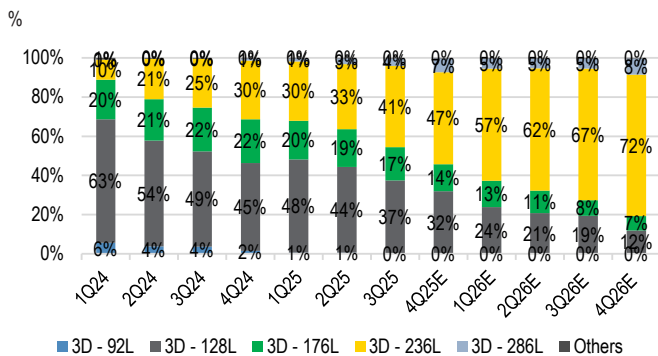
Source: Kioxia & Sandisk company data.

Table 11: Legacy of NAND innovations

Year	Generation	Technology	Capacity
2001	1st	2D NAND	1 Gb (x2-160nm)
2003	2nd	2D NAND	2 Gb (x2-130nm)
2005	3rd	2D NAND	4 Gb (x2-90nm)
2007	4th	2D NAND	8 Gb (x2-70nm)
2009	5th	2D NAND	16 Gb (x3-56nm)
2010	6th	2D NAND	32 Gb (x3-43nm)
2011	7th	2D NAND	64 Gb (x3-32nm)
2013	8th	2D NAND	64 Gb (x3-24nm)
2015	9th	2D NAND	128 Gb (x3-19nm)
2016	10th	2D NAND	128 Gb (x3-17nm)
2017	11th	3D NAND	256 Gb (x3-BICS2 48L)
2018	12th	3D NAND	256 Gb (x3-BICS3 64L)
2019	13th	3D NAND	256 Gb (x3-BICS4 96L)
2020	14th	3D NAND	512 Gb (x3-BICS5 112L)
2021	15th	3D NAND	1 Tb (x3-BICS6 162L)
2023	16th	3D NAND	1 Tb (x3-BICS8 218L)
2025	17th	3D NAND	1 Tb (x3-BICS8 218L)

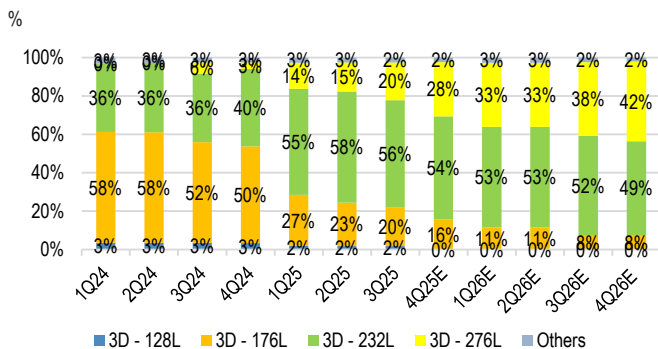
Source: Sandisk 2025 investor day PT.

Figure 113: SEC bit production by layer count



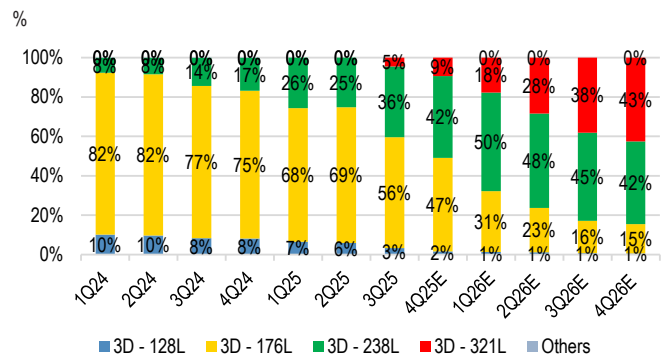
Source: OMDIA.

Figure 115: Micron bit production by layer count



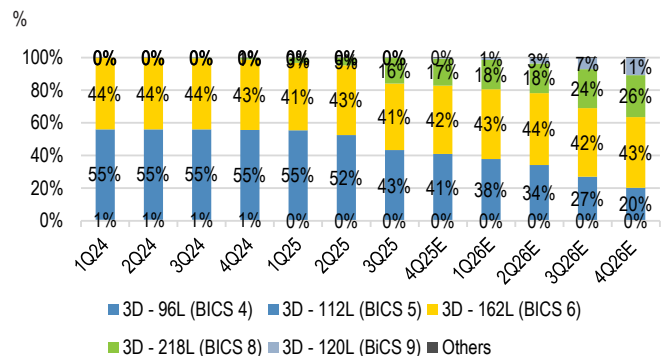
Source: OMDIA.

Figure 114: SK bit production by layer count



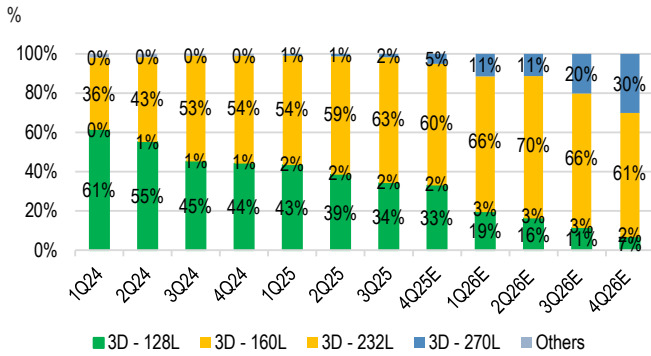
Source: OMDIA.

Figure 116: Kioxia/WD bit production by layer count



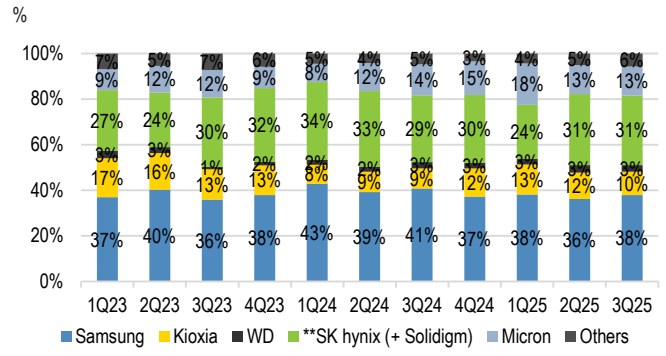
Source: OMDIA.

Figure 117: YMTC bit production by layer count



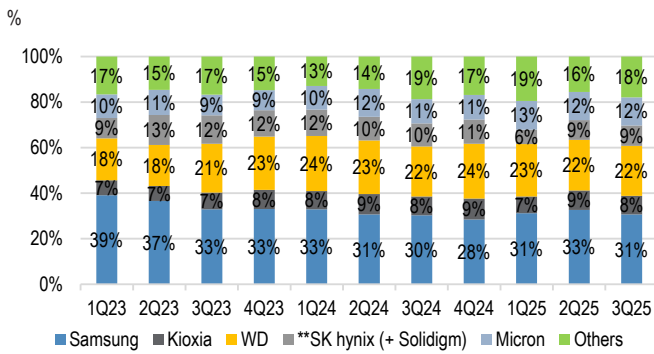
Source: OMDIA.

Figure 118: NAND suppliers M/S in enterprise



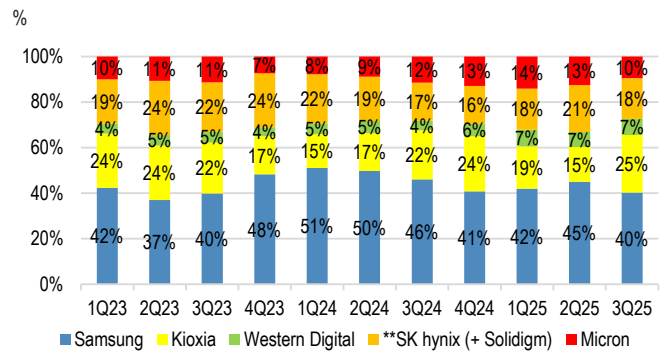
Source: OMDIA.

Figure 119: NAND suppliers M/S in client



Source: OMDIA.

Figure 120: NAND suppliers M/S in mobile



Source: OMDIA.

Kioxia’s BiCS technology

Kioxia’s BiCS (Bit Cost Scaling) technology is a critical and strategically distinct approach in the 3D NAND flash memory landscape. While all major manufacturers have converged on vertical stacking of charge-trap memory cells, Kioxia’s recent adoption of CMOS Directly Bonded to Array (CBA) in its 8th and 9th generation BiCS products represents a significant architectural departure from its peers .

The BiCS process, particularly with the CBA innovation, is critical to Kioxia’s competitive standing by addressing the fundamental trade-off between performance and density in 3D NAND fabrication. The core of the CBA strategy is architectural disaggregation, which involves manufacturing the CMOS peripheral logic and the NAND memory array on two separate, optimized silicon wafers before bonding them together. This separation is crucial because it allows the high-speed CMOS circuitry to be fabricated using advanced, low-temperature logic processes (e.g., 28nm or 14nm) without being subjected to the extreme thermal budget (temperatures exceeding ,1000°C) required for the high-aspect-ratio etching and deposition of the NAND array. This decoupling not only enables higher interface speeds, but also maximizes the bit density per die.Kioxia’s CBA-based BiCS process fundamentally alters the manufacturing flow compared to monolithic approaches (COP/CuA/PUC) (see Figure 111 above for a simplified explanation of the various NAND fabrication processes).

While monolithic designs (V-NAND, D NAND, RG NAND) simplify the overall manufacturing flow by keeping all components on a single wafer, they are constrained by the thermal budget, which limits the performance of the underlying CMOS. Kioxia's choice to add the complexity of wafer bonding is a calculated strategic move to prioritize performance and density scaling, positioning BiCS as a key technology for high-performance applications like enterprise SSDs and AI data centers.

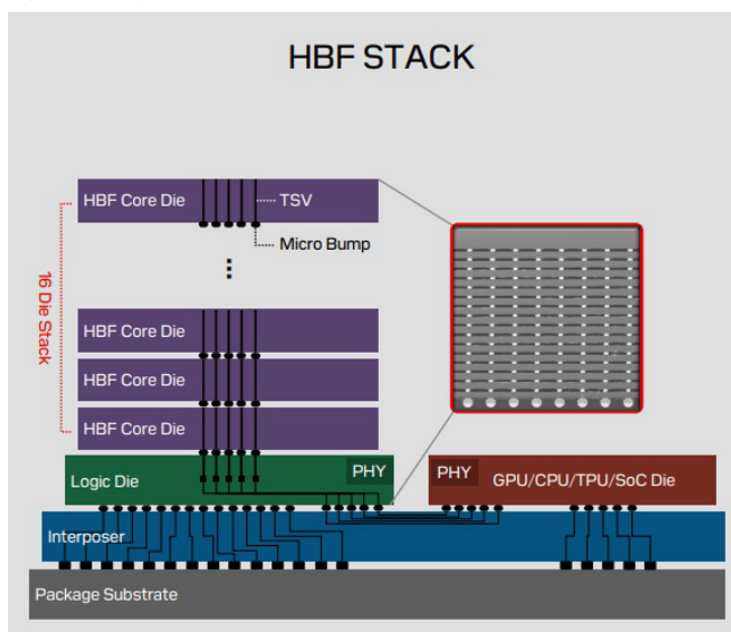
High Bandwidth Flash (HBF)

High Bandwidth Flash is a technology initially introduced by Sandisk which aims to address the growing memory gap for AI and create a new memory standard for intelligent systems by offering a lower-cost, higher-capacity alternative to DRAM-based HBM. This product combines NAND flash's high capacity with High Bandwidth Memory's (HBM) high throughput for **AI inference workloads**. Similar to HBM, this innovation mainly involves stacking 3D-NAND dies using TSV, thereby enabling comparable bandwidth to HBM while providing 8-16 times more capacity at a similar cost, which will potentially allow large AI models to be stored directly on GPU hardware while boosting efficiency.

While development has been ongoing for a while, SanDisk expects to have HBF technology *product detailed concept available by 2H CY2026, and product samples, including the controller device, in the first half of 2027*, thereby ushering in a new paradigm that addresses the "memory wall" problem by increasing memory available to AI accelerators while keeping pace with the demands of growing AI models.

Of note, SanDisk has formed an ecosystem partnership with SK Hynix to standardize HBF technology specifications, which will ensure wider adoption across the industry if the technology proves to deliver the promised performance, compatibility, and scalability benefits for next-generation memory solutions.

Figure 121: High Bandwidth Flash



Source: Sandisk Investor Day.

Critical Challenges in Technology Scaling

As stack heights grow taller, NAND makers face several hurdles highlighted below:

- **High Aspect Ratio Etching** - Drilling uniform memory channels through 30 μm -thick stacks is extremely difficult, as profile deviation—where holes become distorted or narrower at the bottom—can lead to cell failure.
- **Wafer Warpage & Stress** -Stacking hundreds of layers creates massive mechanical stress that can cause wafers to bow or deform by hundreds of microns, necessitating "stress compensation" techniques such as depositing materials on the wafer's backside to flatten it.
- **Word-Line Resistance** -As layers become thinner and the resistance of conductive word lines increases, the industry is transitioning to new materials like Molybdenum (Mo), which has lower resistivity than traditional Tungsten.
- **Cell Efficiency** -Moving the peripheral logic (CMOS) under the memory array (COP/CuA) used to save space, but at 400+ layers, the heat from the logic can damage the memory cells above it.

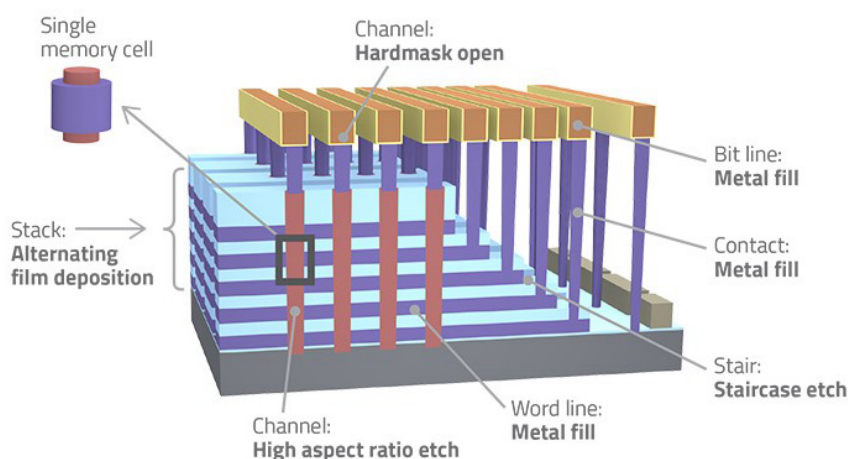
Hybrid Bonding

Hence, NAND makers have to use Hybrid Bonding (wafer-to-wafer copper bonding) to overcome the above challenges. The CMOS logic (peripheral circuits) and the NAND memory array are fabricated on **separate wafers**, which allows each to be optimized independently using the best possible process node (e.g., a 28nm logic node for the controller and a specialized memory node for the array). Because the logic is no longer baked under the memory during the high-heat memory fabrication steps, it performs better and stays cooler. Instead of using traditional "bumps," the two wafers are bonded face-to-face using direct copper pads, which reduces interconnect pitch to **under 1 μm** , providing 10,000x higher I/O density than traditional packaging.

However, while Hybrid Bonding slashes latency by up to **40%** and increases interconnect density by **15x** compared to older solder-bumping methods, it comes with its own challenges. Hybrid bonding can help eliminate some **assembly steps** compared to traditional micro-bump stacking, streamlining the back-end; however, this is offset by the increased amount of time required to etch channel vias, thereby lowering the overall wafer-per-hour (WPH) rate of the memory wafer. The move to hybrid bonding is driving a massive surge in capital expenditure as manufacturers must overhaul both front-end and back-end facilities. For example, **SK Hynix** is aggressively pulling forward hybrid bonding for their V10 (300-layer) products to maintain a competitive edge. Manufacturers must not only invest in ultra-high precision bonders and CMP tools to ensure smooth surfaces for bonding, but there is always a risk of lower yields as defective logic chips may be bonded to functional memory chips.

Figure 122: 3D-NAND memory array

Key Process Steps in 3D NAND Memory Cell Formation



Source: LAM research.

Capital Expenditure Trends

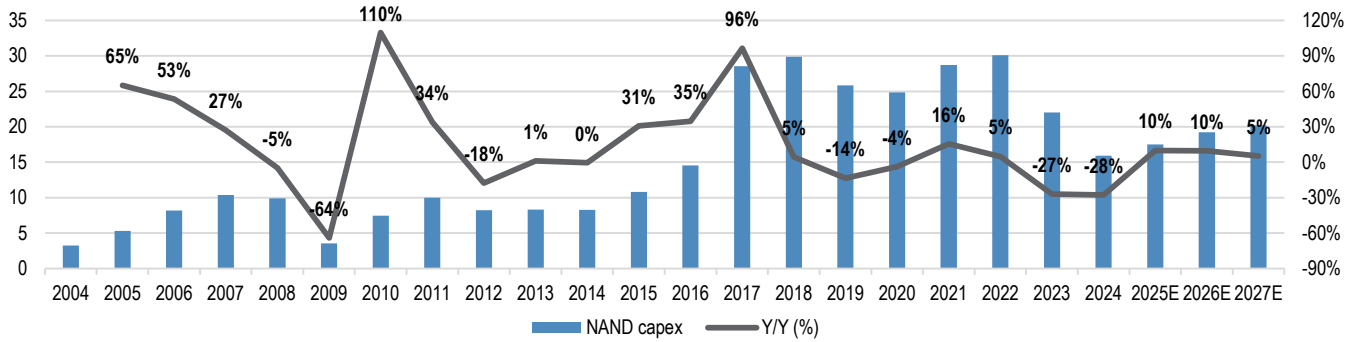
Looking at NAND capital intensity trends for the past 20 years, we observe that capex-to-sales intensity has been extremely volatile with values ranging from 24%-81% as the NAND industry goes through boom and bust cycles often. Given the commodity nature of NAND, NAND makers initially focused on shrinking process nodes (moving from planar to 3D NAND), which required investments in equipment and infrastructure, while currently, they are focused on increasing their layer count, which demands further capital outlays for more complex manufacturing.

Second, the industry has seen periods of high demand (smartphone cycle, etc.) which leads to aggressive capacity additions, followed by oversupply and price crashes, causing swings in capital spending. Hence, the volatility in capital intensity is a result of the NAND industry's need to constantly innovate, respond to market cycles, and manage high fixed costs, all while navigating unpredictable external factors. Of note, we expect NAND capital intensity to stabilize around high-teens % levels (much lower than the last 3/5/7/10 year avg.) over the next 3 years, driven by rising NAND sales and a focus on tech migration rather than capacity additions by major NAND makers.

The current memory super cycle is a function of not only improving demand trends but also supply discipline, in our view, enabled by memory makers' focus on limited wafer growth, coupled with sharply lower capital intensity. The downturn of 2022-2023, when NAND manufacturers recorded significant losses and write-downs, instilled a new focus on profitability and ROIC.

Figure 123: Long-term NAND capex trend

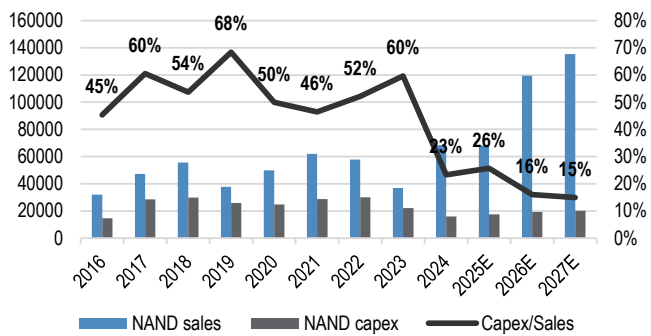
Capex and sales in US\$bn, % - RHS



Source: J.P. Morgan estimates, Company data.

Figure 124: Long-term NAND capex/sales trend

Capex and sales in US\$mn, % - RHS



Source: J.P. Morgan estimates, Company data.

Figure 125: NAND capital intensity comparison across time horizons

	Last 10 yrs	Last 7 yrs	Last 5 yrs	Last 3 yrs	Next 3 yrs
SK Hynix	52%	43%	29%	16%	11%
SEC	44%	44%	43%	40%	13%
Micron	60%	61%	59%	53%	29%
Kioxia	30%	29%	27%	25%	10%
YMTC	n.a	n.a	168%	166%	57%

Source: J.P. Morgan estimates, Company data.

Share Price Analysis

Memory Industry Market Cap comparison since 2025

Despite the introduction of DeepSeek in China as well as Liberation Day scares across the globe, memory stocks have been on an upward trajectory ever since the turn of the last year (Jan25). While 1Q25 earnings were rather subdued due to air pockets in HBM and eSSD sales, memory makers rallied with the pure play DRAM makers (NYT) outperforming the NAND and diversified memory makers. This outperformance was mainly driven by investor expectations of DDR4 EOL, which led to an unprecedented DDR4 spot price rally.

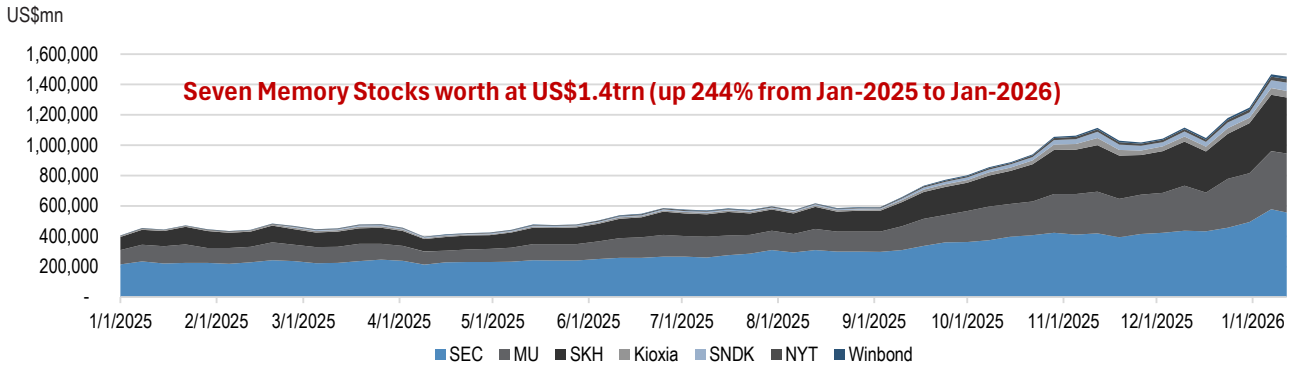
Second, as investor concerns on the sustainability of AI capex were quickly alleviated, the diversified memory makers (SKH, SEC) started rallying as tight HBM S/D played a critical role in reducing conventional DRAM capacity, which further tightened overall memory S/D dynamics. While initially NAND had limited exposure to AI (as CE drives 60-70% of NAND B/G), the transition from training to inference workloads, coupled with supply discipline from NAND makers, led to a sustained price rally in NAND spot prices, as a result driving pure-play NAND makers' stock prices.

Of note, since the start of 2025, the overall memory market market-cap has grown 242% on average (growing from US\$405bn to US\$1.39trn), with diversified memory makers rallying 265% on average, while pure-play DRAM and NAND makers have rallied 680% and 649%, respectively.

While we expect ASP hikes-driven EPS upgrades for memory stocks across Asia/U.S to continue in the near term, we believe, with fairly high expectations on pricing over the past few months (above historical peak valuation prior to the current up-cycle), the share reaction to potential beats and raises may not be as strong as in the CY3Q25 results season. However, with memory makers already having sold out volumes for 2026, coupled with continued tightness across HBM/eSSDs, we expect pricing to remain elevated. Within the large-cap Asian memory space, SEC (OW) > SKH (OW) is our near-term pecking order (vs mid- to long-term pecking order unchanged: SKH > SEC). We remain OW on Winbond and Neutral on NYT among our commodity memory coverage. We also like MU (OW) – U.S. memory with rising AI exposure.

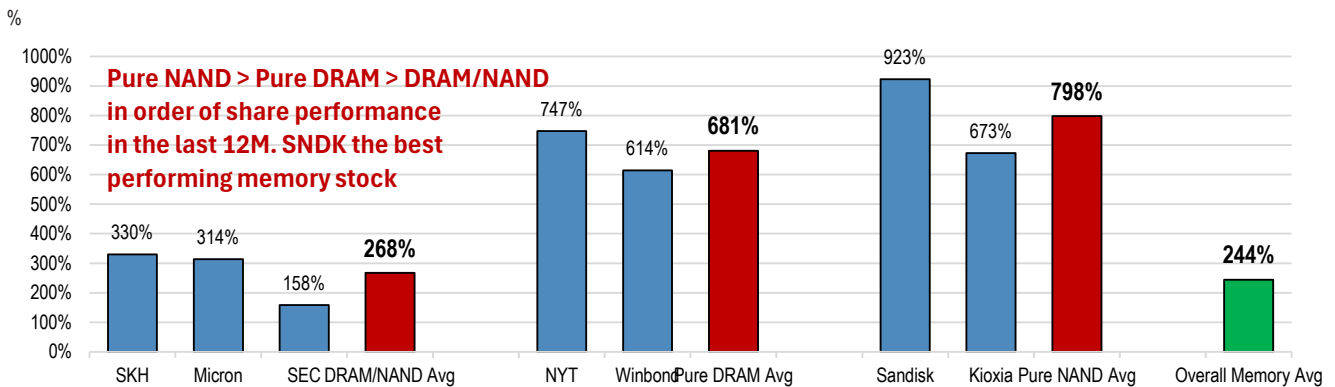
On the NAND side, the surge in demand is largely fueled by the rapid expansion of data centers and AI infrastructure, as hyperscalers, cloud service providers, and AI research orgs continue to roll out storage-heavy systems. In response, memory makers are focusing on tech migration rather than capacity additions, which will drive lower levels of capital intensity and restrain growth in wafer output. Meanwhile, the inability of the HDD supply chain to meet AI-related demand is providing further tailwinds to eSSD demand. With much of the available capacity for 2025-2026 – and even into 2027 – already committed through long-term contracts, we believe NAND bit demand will continue to outpace bit supply, thereby keeping the overall NAND S/D demand balanced in 2026. Among NAND makers in Asia, Kioxia (OW) is our top pick, while we remain Neutral on Sandisk due to its limited exposure to AI-driven eSSD demand explosion.

Figure 126: Memory Market cap trend since Jan'25



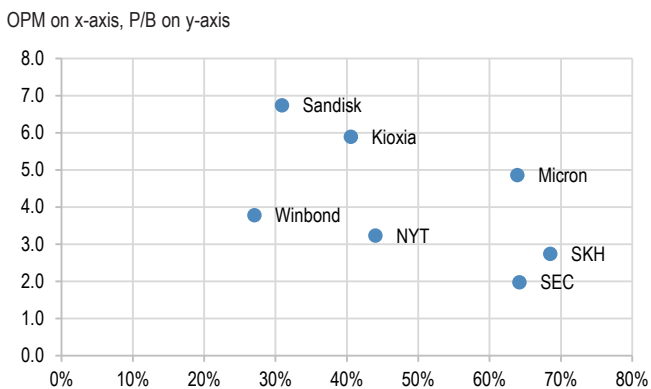
Source: Bloomberg Finance L.P.

Figure 127: Memory Stock Price performance since Jan'25



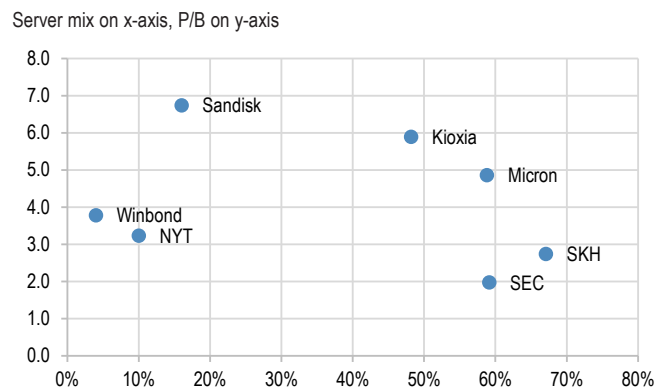
Source: Bloomberg Finance L.P.

Figure 128: 2026 OPM vs 12M FWD P/B



Source: J.P. Morgan estimates, company data, Bloomberg Finance L.P.
 Note: Considered total memory for SEC, SKH and Micron, just DRAM for NYT & Winbond and just NAND for Sandisk & Kioxia. Note: Data as of 22nd Jan, 2026.

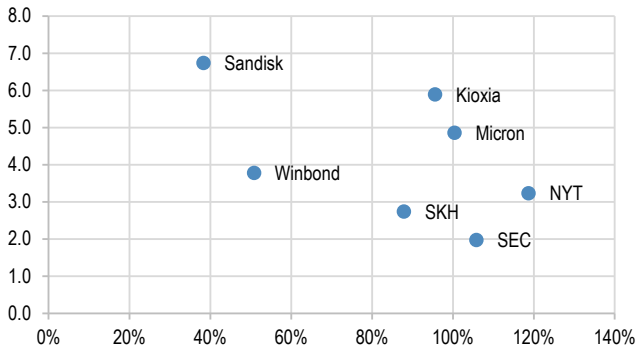
Figure 129: 2026 server mix vs 12M FWD P/B



Source: J.P. Morgan estimates, Company data, Bloomberg Finance L.P.
 Note: Considered total memory for SEC, SKH and Micron, just DRAM for NYT & Winbond and just NAND for Sandisk & Kioxia. Note: Data as of 22nd Jan, 2026.

Figure 130: 2026 Sales growth (Y/Y) vs 12M FWD P/B

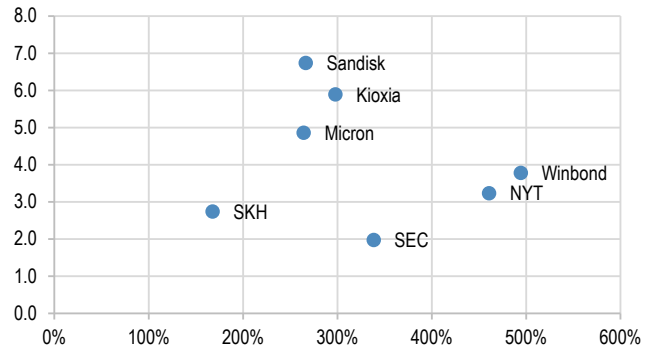
Sales mix on x-axis, P/B on y-axis



Source: J.P. Morgan estimates, Company data, Bloomberg Finance L.P.
 Note: Considered total memory for SEC, SKH and Micron, just DRAM for NYT & Winbond and just NAND for Sandisk & Kioxia. Note: Data as of 22nd Jan, 2026.

Figure 131: 2026 OP growth (Y/Y) vs 12M FWD P/B

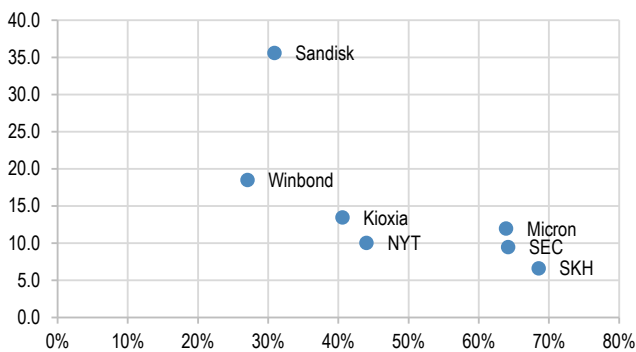
OP growth on x-axis, P/B on y-axis



Source: J.P. Morgan estimates, Company data, Bloomberg Finance L.P.
 Note: Considered total memory for SEC, SKH and Micron, just DRAM for NYT & Winbond and just NAND for Sandisk & Kioxia. Note: Data as of 22nd Jan, 2026.

Figure 132: 2026 OPM vs 12M FWD P/E

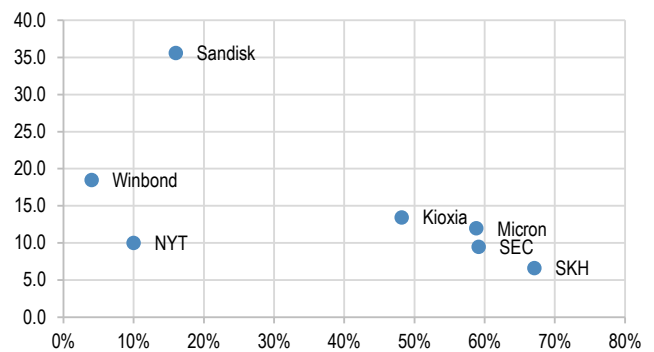
OPM on x-axis, P/E on y-axis



Source: J.P. Morgan estimates, company data, Bloomberg Finance L.P.
 Note: Considered total memory for SEC, SKH and Micron, just DRAM for NYT & Winbond and just NAND for Sandisk & Kioxia. Note: Data as of 22nd Jan, 2026.

Figure 133: 2026 server mix vs 12M FWD P/E

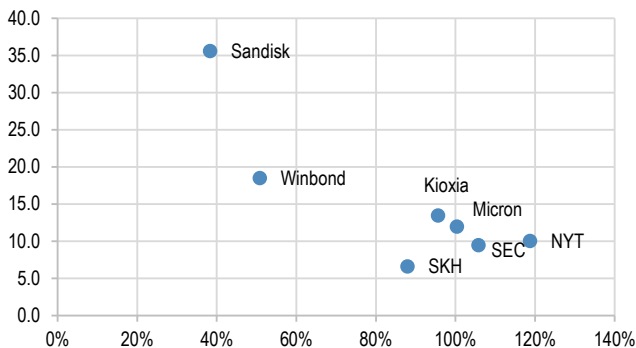
Server mix on x-axis, P/E on y-axis



Source: J.P. Morgan estimates, Company data, Bloomberg Finance L.P.
 Note: Considered total memory for SEC, SKH and Micron, just DRAM for NYT & Winbond and just NAND for Sandisk & Kioxia. Note: Data as of 22nd Jan, 2026.

Figure 134: 2026 OP growth (Y/Y) vs 12M FWD P/E

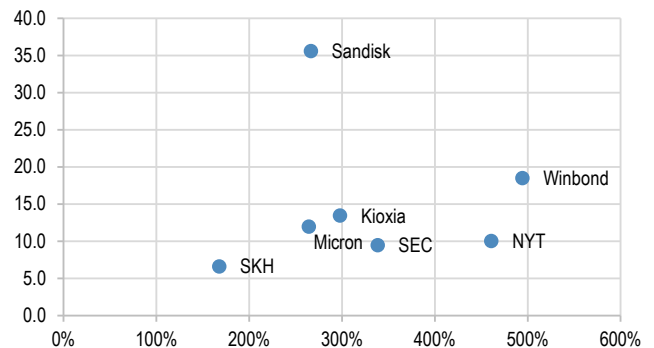
OP growth on x-axis, P/E on y-axis



Source: J.P. Morgan estimates, Company data, Bloomberg Finance L.P.
 Note: Considered total memory for SEC, SKH and Micron, just DRAM for NYT & Winbond and just NAND for Sandisk & Kioxia. Note: Data as of 22nd Jan, 2026.

Figure 135: 2026 Sales growth (Y/Y) vs 12M FWD P/E

Sales mix on x-axis, P/E on y-axis



Source: J.P. Morgan estimates, Company data, Bloomberg Finance L.P.
 Note: Considered total memory for SEC, SKH and Micron, just DRAM for NYT & Winbond and just NAND for Sandisk & Kioxia. Note: Data as of 22nd Jan, 2026.

Table 12: Broader Memory Value Chain Valuation Table

Company	Ticker	Price (LC)	Market Cap (US\$ M)	Revenue			Revenue growth Y/Y			P/E(x)			EPS growth Y/Y			P/B(x)			ROE (%)			YTD perf. (%)
				FY25E	FY26E	FY27E	FY25E	FY26E	FY27E	FY25E	FY26E	FY27E	FY25E	FY26E	FY27E	FY25E	FY26E	FY27E	FY25E	FY26E	FY27E	
Pure DRAM																						
Nanya Technology Corp	2408 TT	267	26,113	1,986	5,552	5,946	87%	180%	7%	33.4	9.7	9.9	-151%	3364%	-3%	5.0	3.2	2.6	2%	35%	28%	38.1
Winbond Electronics Corp	2344 TT	105	14,871	2,787	4,164	5,888	10%	49%	41%	117.3	18.5	10.6	311%	534%	74%	4.7	3.8	2.6	4%	27%	29%	26.5
Average										225.8	14.1	10.3	80%	1949%	36%	4.8	3.5	2.6				32.3
Pure NAND																						
Sandisk Corp/DE	SNDK US	501	73,466	7,271	11,035	14,190	9%	52%	29%	185.7	35.6	18.0	n.a	422%	97%	8.0	6.6	5.1	3%	22%	29%	111.2
Kioxia Holdings Corp	285A JP	17,910	61,426	12,303	18,397	18,434	65%	50%	0%	33.7	13.4	12.0	n.a	152%	12%	9.4	5.9	4.2	33%	63%	41%	71.6
Average										109.7	24.5	15.0	n.a	287%	55%	8.7	6.2	4.7				91.4
Memory																						
Samsung Electronics Co Ltd	005930 KS	154,100	620,475	72,063	114,772	138,286	16%	59%	20%	24.5	9.7	8.5	28%	153%	14%	2.5	2.0	1.7	10%	22%	21%	28.0
SK hynix Inc	000660 KS	760,000	376,334	64,534	114,424	137,208	33%	77%	20%	13.3	6.7	5.7	131%	99%	18%	4.8	2.8	1.8	44%	54%	38%	16.6
Micron Technology Inc	MU US	389	437,947	37,177	74,628	93,806	48%	101%	26%	48.2	12.0	9.2	558%	303%	30%	8.3	4.9	3.2	17%	48%	41%	36.3
Average										28.7	9.4	7.8	345%	201%	24%	5.2	3.2	2.2				27.0
HDD																						
Western Digital Corp	WDC US	242	82,705	9,383	11,914	13,901	49%	27%	17%	46.0	30.5	23.7	-1041%	51%	28%	15.1	10.2	8.2	25%	43%	41%	40.4
Seagate Technology Holdings PL	STX US	344	73,511	9,073	11,101	13,008	38%	22%	17%	43.3	29.3	21.5	693%	48%	36%	n.a	82.4	24.5	n.a	-331%	228%	25.0
Average										44.7	29.9	22.6	-174%	49%	32%	15.1	46.3	16.3				32.7
Controllers																						
Phison Electronics Corp	8299 TT	2,055	13,515	2,256	3,261	3,742	23%	45%	15%	57.7	28.2	28.5	14%	105%	-1%	8.2	6.9	6.3	14%	27%	24%	41.7
Marvell Technology Inc	MRVL US	83	70,011	5,753	8,181	9,991	4%	42%	22%	52.8	29.1	23.0	3%	82%	26%	5.3	4.9	4.4	-1%	1%	10%	(2.9)
Silicon Motion Technology Corp	SIMO US	118	4,004	868	1,010	1,125	8%	16%	11%	33.3	25.0	19.9	8%	33%	25%	4.6	4.2	3.6	13%	16%	17%	27.1
Average										48.0	27.4	23.8	6%	57%	26%	6.0	5.3	4.8				22.0
WFE/SPE																						
Applied Materials Inc	AMAT US	325	257,897	28,240	28,953	33,026	4%	3%	14%	34.8	33.7	28.0	10%	3%	21%	13.5	11.3	10.0	38%	34%	36%	26.6
KLA Corp	KLAC US	1,520	199,716	12,058	13,099	14,948	23%	9%	14%	46.8	42.3	35.3	40%	11%	20%	49.0	33.8	25.5	110%	88%	83%	25.1
Lam Research Corp	LRXC US	228	286,865	18,262	21,381	24,477	23%	17%	14%	56.9	46.7	38.9	35%	22%	20%	28.6	24.6	18.9	54%	58%	68%	33.4
Tokyo Electron Ltd	8035 JT	42,500	126,264	15,305	17,322	19,072	21%	13%	10%	39.3	32.8	27.9	-7%	20%	17%	9.4	8.4	7.3	25%	27%	28%	23.8
ASM International NV	ASM NA	728	42,000	3,705	4,073	4,873	17%	10%	20%	52.7	43.7	34.2	4%	21%	28%	8.8	7.7	6.5	18%	20%	22%	40.7
Teradyne Inc	TER US	232	36,316	3,070	3,799	4,441	9%	24%	17%	66.0	44.4	33.9	11%	49%	31%	12.4	11.1	8.8	19%	27%	30%	19.8
Advantest Corp	6857 JT	22,850	110,276	5,260	6,124	7,316	56%	16%	19%	97.4	58.3	46.8	162%	67%	25%	32.2	25.4	19.2	36%	48%	50%	16.4
Average										46.2	40.9	34.0	86%	58%	28%	30.4	23.2	18.1				26.5

Source: Bloomberg Finance L.P. Note: Data as of 22 Jan, 2026.

Companies Discussed in This Report (all prices in this report as of market close on 23 January 2026, unless otherwise indicated)

KIOXIA Holdings (285A)(285A.T/¥17,335/OW), Micron Technology(MU/\$397.58[22 January 2026]/OW), Nanya Technology(2408.TW/NT\$271.50/N), SK hynix(000660.KS/W767,000/OW), Samsung Electronics(005930.KS/W151,700/OW), Sandisk(SNDK/\$503.44[22 January 2026]/N), Silicon Motion(SIMO/\$115.27[22 January 2026]/OW), Tokyo Electron (8035) (8035.T/¥41,720/OW), Winbond(2344.TW/NT\$103.00/OW)

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KIOXIA Holdings (285A) (285A.T, 285A JP) Price Chart



Date	Rating	Price (Y)	Price Target (Y)
23-Jan-26	OW	17910	25,000

Source: Bloomberg Finance L.P. and J.P. Morgan; price data adjusted for stock splits and dividends.

Samsung Electronics (005930.KS, 005930 KS) Price Chart



Date	Rating	Price (W)	Price Target (W)
15-Jun-23	OW	71900	90,000
01-Feb-24	OW	72700	95,000
03-Apr-24	OW	85000	110,000
03-Jul-24	OW	81800	120,000
08-Sep-24	OW	68900	100,000
08-Oct-24	OW	61000	84,000
31-Oct-24	OW	59100	83,000
10-Dec-24	N	53400	60,000
03-Apr-25	OW	58800	74,000
30-Apr-25	OW	55800	68,000
02-Jul-25	OW	60200	71,000
01-Aug-25	OW	71400	84,000
25-Sep-25	OW	85400	100,000
27-Oct-25	OW	98900	135,000
30-Oct-25	OW	101700	140,000
14-Dec-25	OW	108500	160,000
16-Jan-26	OW	145000	200,000

Source: Bloomberg Finance L.P. and J.P. Morgan; price data adjusted for stock splits and dividends. Initiated coverage Oct 09, 2011. All share prices are as of market close on the previous business day.

SK hynix (000660.KS, 000660 KS) Price Chart



Source: Bloomberg Finance L.P. and J.P. Morgan; price data adjusted for stock splits and dividends. Initiated coverage Dec 31, 2000. All share prices are as of market close on the previous business day.

Date	Rating	Price (W)	Price Target (W)
26-Apr-23	OW	85500	120,000
12-Jun-23	OW	115400	150,000
07-Nov-23	OW	133000	160,000
25-Jan-24	OW	141500	175,000
22-Feb-24	OW	149000	185,000
28-Mar-24	OW	181200	260,000
16-Jul-24	OW	230000	300,000
08-Sep-24	OW	156400	240,000
24-Oct-24	OW	196000	260,000
10-Dec-24	OW	168900	210,000
23-Jan-25	OW	225500	280,000
03-Apr-25	OW	197900	300,000
24-Apr-25	OW	181000	285,000
25-Jun-25	OW	278500	360,000
24-Sep-25	OW	361000	460,000
23-Oct-25	OW	481000	650,000
29-Oct-25	OW	519000	700,000
14-Dec-25	OW	571000	800,000
16-Jan-26	OW	756000	1,000,000

Tokyo Electron (8035) (8035.T, 8035 JP) Price Chart



Source: Bloomberg Finance L.P. and J.P. Morgan; price data adjusted for stock splits and dividends. Initiated coverage Apr 04, 2001. All share prices are as of market close on the previous business day.

Date	Rating	Price (Y)	Price Target (Y)
11-Apr-23	OW	15325	20,000
27-Sep-23	OW	20165	24,000
09-Feb-24	OW	29435	34,200
09-Jul-24	OW	36040	41,000
11-Dec-24	OW	24600	35,000
13-Jun-25	OW	25000	31,000
12-Sep-25	OW	21405	26,000
08-Nov-25	OW	32800	38,000
10-Jan-26	OW	37910	45,000

The chart(s) show J.P. Morgan's continuing coverage of the stocks; the current analysts may or may not have covered it over the entire period. J.P. Morgan ratings or designations: OW = Overweight, N= Neutral, UW = Underweight, NR = Not Rated

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